EE 0147: Analog and Mixed-Signal MOS Integrated Circuit Design
Department of Electrical and Computer Engineering
Tufts University
Spring 2005

Lecture	*Lab*
Halligan 106	Halligan 118
Time: Tuesdays, Thursdays 7:00-8:15pm	Time: TBA

Pre-requisites:

Electrical Circuit Analysis –Nodal analysis, Loop analysis, 1st and 2nd order circuit analysis, Diodes, BJT, MOS transistor basics, Small signal analysis, Bode plots
System Level Analysis – S-transform, Z- transform analysis
CAD tools – SPICE/SPECTRE simulation tool, CADENCE design environment
(*Please seek permission from the instructor if you do not satisfy the above prerequisites*)

Instructor	*Teaching Assistant*
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Textbook:

Design of Analog CMOS Integrated Circuits
Behzad Razavi
McGraw-Hill, ISBN 0-07-238032-2
(*Class notes will accompany the textbook)*

References:

1. Analog Integrated Circuit Design, David A. Johns and Ken Martin, John Wiley and Sons, ISBN 0-471-14448-7
2. CMOS Analog Circuit Design, Phillip E. Allen and Douglas R. Holdberg, Oxford University Press, ISBN 0-19-511644-5
3. Analysis and Design of Analog Integrated Circuits, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, John Wiley and Sons, ISBN 0-471-32168-0

Course Description:
This course will cover topics on analog and mixed-signal circuit design in a CMOS Integrated Circuits (CMOS IC) technology. Analog design differs from digital design primarily in the nature of the signals being processed. In digital design, the circuits stabilize to one of two signal levels – high or low. However in analog design, the circuits work on the entire range of the signal. Some examples of analog circuits are amplifiers, filters, oscillators, voltage and current references, multipliers, rectifiers etc.

Due to the insatiable need for high speed and ubiquitous computing fueled by growth of computers, PDAs and cell phones, the digital IC industry has been the center of unparalleled growth in the last three decades. However the analog IC industry did not lack behind. Since the real world is analog, there is a growing need for faster, low power, wide dynamic range, and high precision analog circuits to interface with the faster digital world. Moreover mixed-signal systems which have both digital and analog systems on the same substrates offer opportunities for system on chip implementation, which greatly reduce cost and foster true integration. Some examples of mixed-signal circuits and systems include analog to digital converters, digital to analog converters, radio frequency transceivers, embedded controllers etc.

In this course we will focus on analog and mixed-signal designs on a digital CMOS process. The course will begin with reviewing the foundations needed to study advanced topics – MOS transistor theory, common source/emitter and common gate, common drain amplifiers, current mirrors, feedback in analog circuits, differential pair and reference circuit design. In the second quarter, we will cover design of operational amplifiers, and study the effect of noise and offsets. The third quarter will cover advanced topics in continuous time filters and switched capacitor circuits, and lastly we will cover some basics of analog to digital and digital to analog converter design.

Schedule:
The preliminary schedule for the class is given below and is flexible.

1. Introduction – 1/2 week
2. Basics of MOS Transistor theory – 1 week
3. Single Stage Amplifiers – 1-1/2 weeks
4. Differential Amplifiers and active and passive loads– 1-1/2 weeks
5. Frequency response of single stage and differential amplifiers – 2 weeks
6. Noise and Offset Analysis – 1week

7. Feedback – 1 week
8. Operational amplifiers – 2 weeks
9. Continuous time filters – 1 week
10. Switched Capacitor Circuits including non ideal effects– 2 weeks
11. Advanced Topics – remaining time

Structure:
Class notes will be posted online after every class. Students will benefit from *integrated labs and homeworks*. All the labs will use the CADENCE design environment. Some of the labs will also include designing layouts in Cadence. There will be *two exams*, *and a final project* in the course. The final project will require submission of a paper in the IEEE journal format. Additional notes/materials accompanying the final paper to include detailed design simulation results in the form of an "Appendix" will be asked. The final projects will require literature review and incorporation of novel circuit design concepts. The projects will be submitted to MOSIS for fabrication. We plan to use a state of the art TSMC 0.18u CMOS process available through MOSIS for design purposes. The deadline for chip submission to MOSIS is May 16th 2005. Successful project outcomes will be submitted to leading international conferences and journals.

A normalized peer review process will be introduced in the class to improve the learning experience. In a peer review process, every student will be required to grade the lab and homework reports of others assigned at random. The process enables "synergistic learning", and "fosters critical thinking". More so, it makes learning a fun experience, where students control their own destiny in the class. The instructor and the TA will moderate the peer review process.

Grading Policy:
Homework/Labs 20%
Midterm 1 25%
Midterm 2 25%
Final Project 30%

Class Policy:
1. In-class and web-based discussion is encouraged and will be viewed favorably.
2. *Best 5* of all assignments (around 7 may be assigned) will be counted towards your final grade.
3. A late submission of any assignment will get *zero* credit.

4. No make-up is allowed for any exams. Only under serious circumstances and with proper proof, an alternative arrangement at the discretion of the instructor will be made.
5. Discussions for labs are highly encouraged. However the submission must include work in author's own words. *If you seek help, please cite your sources, or else it will be considered cheating and a strict disciplinary action may be taken by the school.*
6. For take-home exams, the exam is closed-books and notes. Students are not allowed to seek help from anyone, or from anywhere.
7. Any dispute during the peer review process will be settled by the instructor.
8. The instructor reserves the right to change the grading policy, the individual grades of the students, course syllabus and the classroom policies at any stage during the class.
9. All grades are final and cannot be disputed.