Name: _____

EE 201 Problem Set 2 Due Tuesday March 6, at class time (1:30pm)

After solving the problems, look at the solutions posted on the course website and categorize your work for each problem on the following scale:

- • Completely correct
- \bullet Nearly correct, but made a small mathematical or copying error
- \bigcirc Solved part of the problem correctly
- • Started some work in the right direction
- \bigcirc Incorrect, or didn't even know where to start on the problem
- Include a question mark (?) in addition to one of the above symbols if you don't feel like you understand the question or the solution well enough to make a definite judgement.

Problems with an asterisk (*) are optional.

1.a	1.b	$1.c^*$	1.d	$1.e^{*}$	2	3.a	3.b	$3.c^*$	$3.d^*$	4.a	$4.b^{*}$	4.c

What questions do you have about these concepts and skills?

What things are you uncertain about (even if you don't have a specific question)?

Approximately how long did it take you to complete the homework?

How long did you take going over the solutions and writing this reflection?

Turn in this self-assessment sheet on Gradescope. You do not need to turn in anything else, although we're happy to look at your work if you have questions!

Problem 1: Logic minimization

Minimize the truth tables and logic functions below.

(a) $\overline{A}BC + \overline{A}B\overline{C} + \overline{A}C\overline{D} + AB\overline{C} + BCD$

(b) $\overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} \overline{C} D + \overline{A} \overline{B} \overline{C} D + \overline{A} \overline{B} \overline{C} \overline{D} + \overline{A} \overline{B} \overline{C} D + \overline{A} \overline{B} \overline{C} D$

Α	В	С	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	Х
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	X
	A 0 0 0 1 1 1 1 1	A B 0 0 0 1 0 1 1 0 1 1 1 1 1 1 1 1	A B C 0 0 0 0 1 0 0 1 1 1 0 0 1 0 1 1 0 1 1 1 0 1 1 1 1 1 1

	А	В	С	D	Y
	0	0	0	0	1
	0	0	0	1	1
	0	0	1	0	0
	0	0	1	1	0
	0	1	0	0	1
	0	1	0	1	X
(-)	0	1	1	0	0
(d)	0	1	1	1	0
	1	0	0	0	0
	1	0	0	1	Х
	1	0	1	0	1
	1	0	1	1	0
	1	1	0	0	0
	1	1	0	1	X
	1	1	1	0	1
	1	1	1	1	1

	А	В	С	D	Y
	0	0	0	0	1
	0	0	0	1	0
	0	0	1	0	0
	0	0	1	1	Х
	0	1	0	0	1
	0	1	0	1	1
	0	1	1	0	0
(e)	0	1	1	1	1
	1	0	0	0	X
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	1	1
	1	1	0	0	0
	1	1	0	1	Х
	1	1	1	0	1
	1	1	1	1	0

Problem 2: Gate implementation

Implement the equation $Y = A\overline{B} + BC$ using only NAND gates (no inverters, just NANDs):

Problem 3: Multiplexers

(a) Implement the equation $Y = A\overline{C} + \overline{A}C + \overline{B}C$ using an 8:1 multiplexer.

(b) Write a truth table for this circuit, showing the output Y as a function of the inputs A, B, and C.



(c) Draw a logic diagram showing how you could implement the equation $Y = A \oplus B$ using only 2:1 multiplexers. *Hint: It might help to first draw how you could implement this with a 4:1 multiplexer.*

(d) Draw a logic diagram for a circuit with the following behavior:

- When V is low, the output signal is simply the input: Y = A.
- When V is high, the output signal is inverted : $Y = \overline{A}$.

Write a truth table for Y in terms of A and V. What do you notice?

Gate	$t_{pd} (ps)$	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40

(a) Determine the propagation delay and contamination delay of the circuit in the figure below. Use the gate delays given in the table above.



Gate	$t_{pd} (ps)$	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40

(b) Determine the propagation delay and contamination delay of the circuit in the figure below. Use the gate delays given in the table above.



Redesign the circuit so that it runs faster (i.e., lower propagation delay), using the gates in the table above. There are multiple ways to speed it up!

(c) Below is a section of a carry-lookahead adder with a block size of 2. For each of the three outputs $(R_0, R_1 \text{ and } C_{cout})$, highlight the critical path. Use the gate delays given in the table above.



Practice Problems - For review

These are selected problems from the textbook (at the end of each chapter) which may be helpful for practice and review. The answers to these problems are online at https://booksite.elsevier.com/9780128000564/solutions.php.

- 2.17 (simplifying equations, drawing circuits)
- 2.27 (bubble pushing)
- 2.31 (minimizing with don't-cares)
- 2.35 (writing and minimizing equations, drawing circuits)