# **EE 201:** More sequential logic in SystemVerilog

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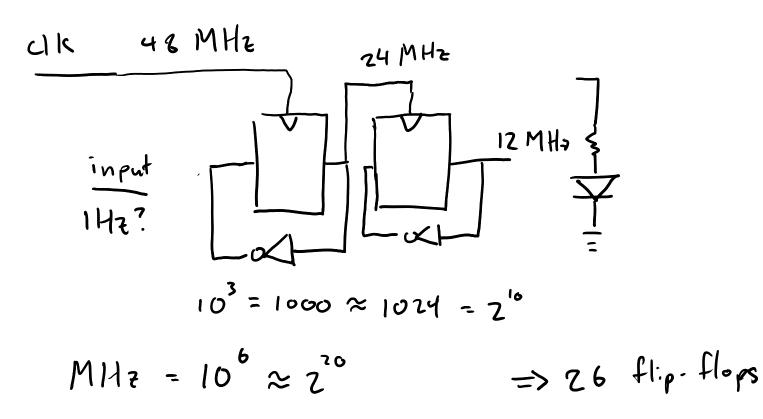
### By the end of class today, you should be able to:

- Build a design for an FPGA from HDL to bitstream
- Build slightly more complicated sequential circuits using SystemVerilog

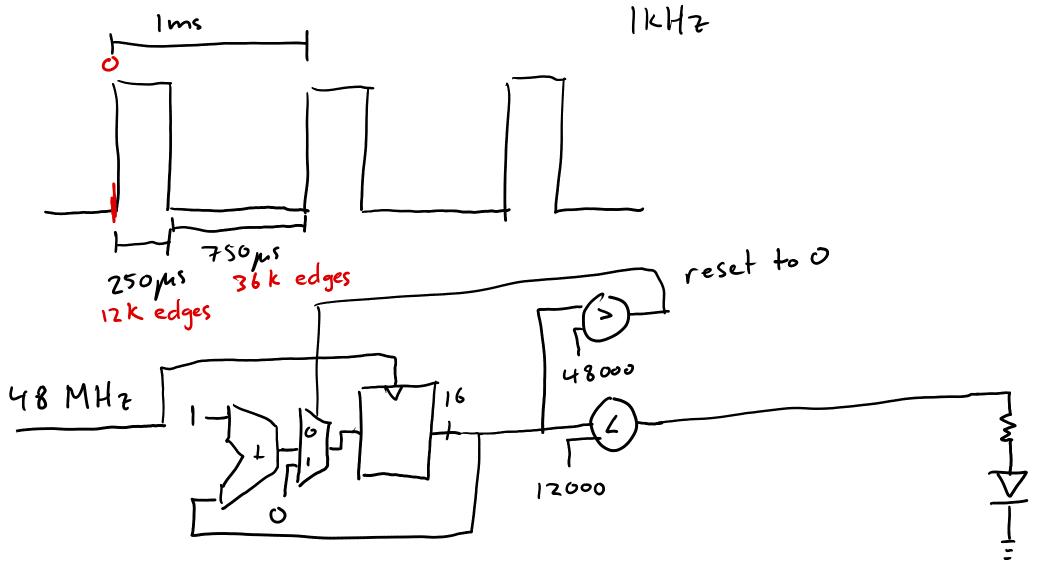
# Blinking an LED?

$$\sim 1H_{z}$$

Design a circuit to blink an LED at a rate humans can see. Assume your input clock runs at 48MHz.



#### **PWM controller**



#### Loadable counter

### **FPGA toolchains**

See link on course website

## For Thursday

- 1. Read book (3.4, 4.6)
- 2. Complete HW 3 if you haven't