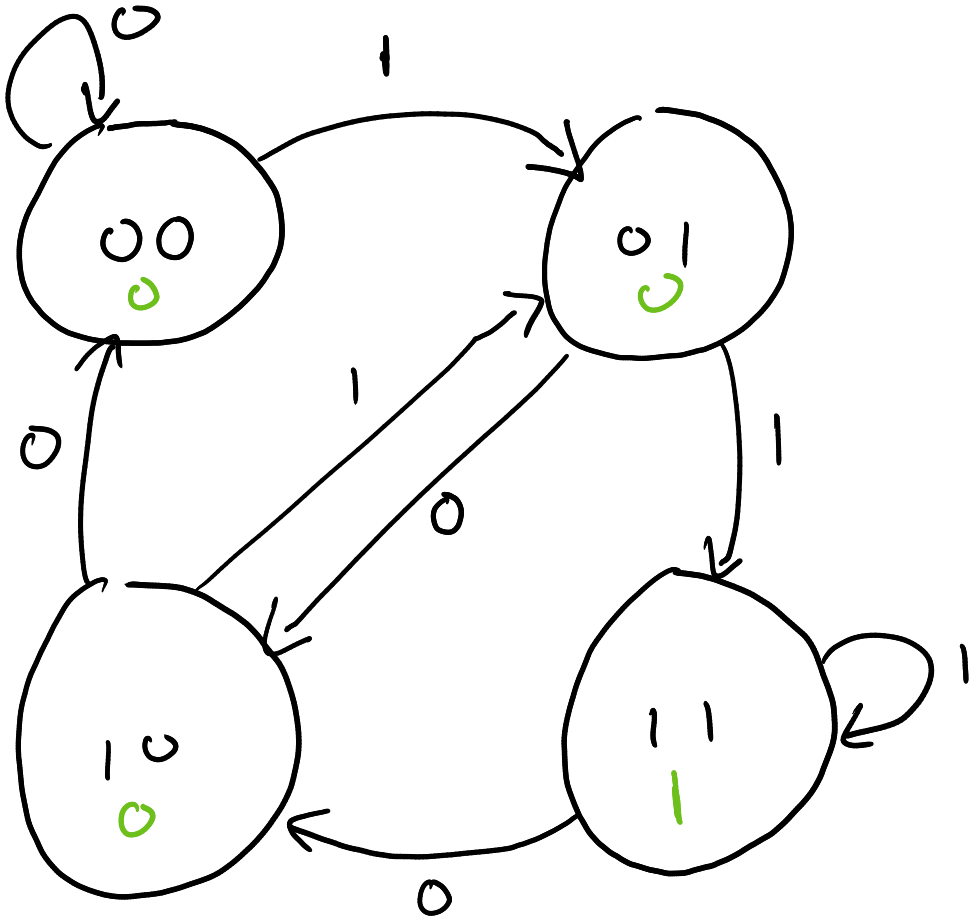
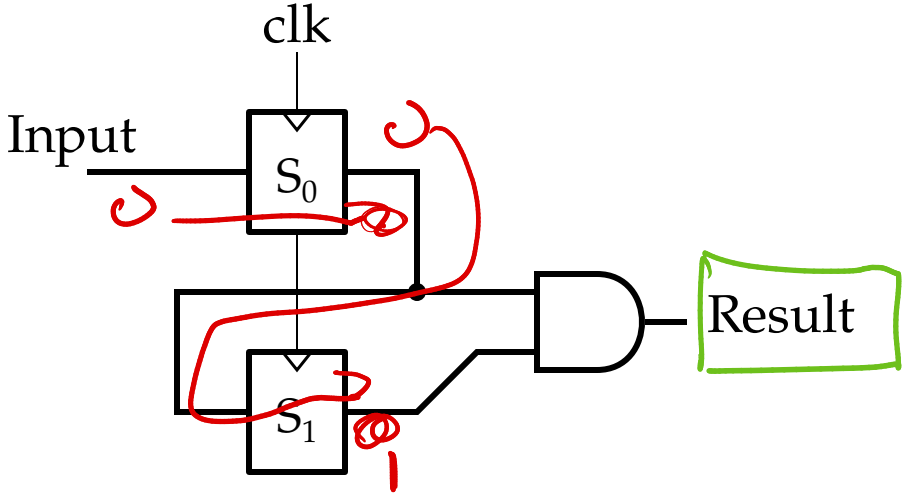
Warmup

Draw a state diagram for the circuit below:

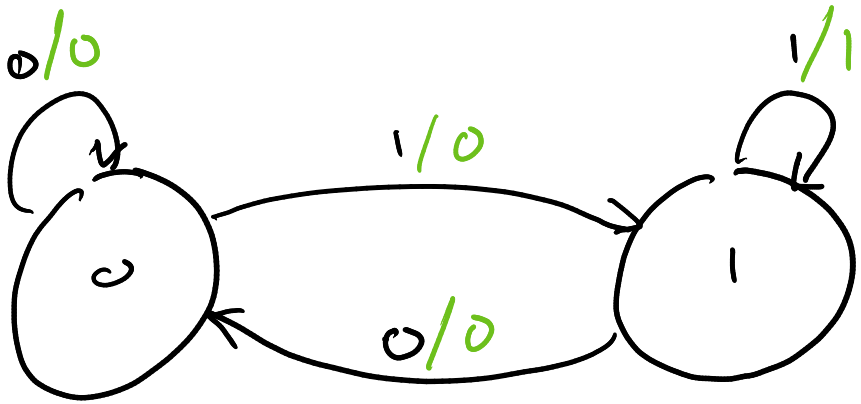
If it helps, assume that both FFs are 0, and work from there

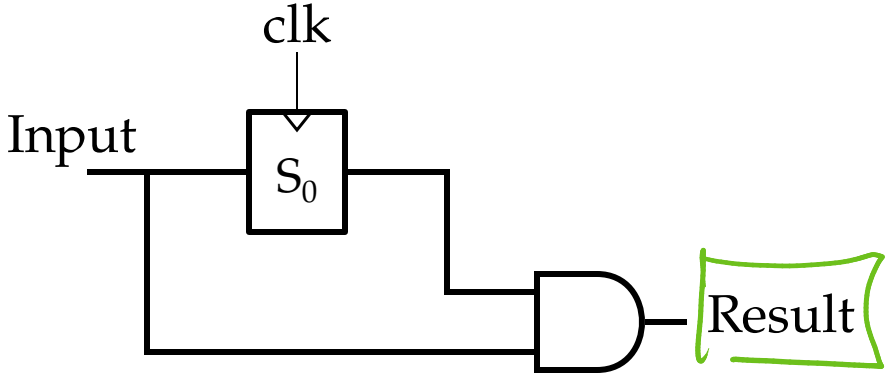




Warmup

What about this circuit?





EE 201: State machines, part 2

Steven Bell

5 March 2024

Tufts UNIVERSITY

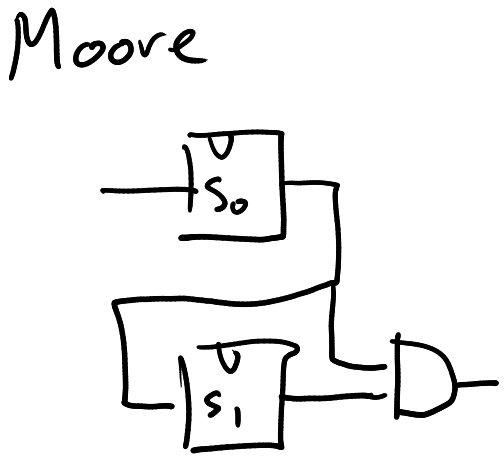
Logistics

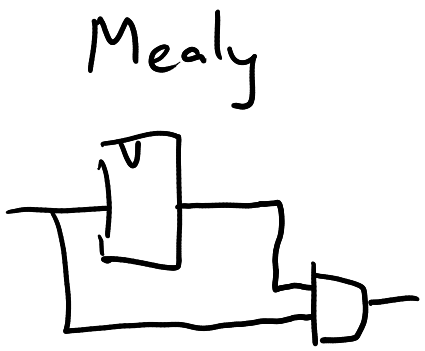
- Exam is March 14 (Thursday before break)

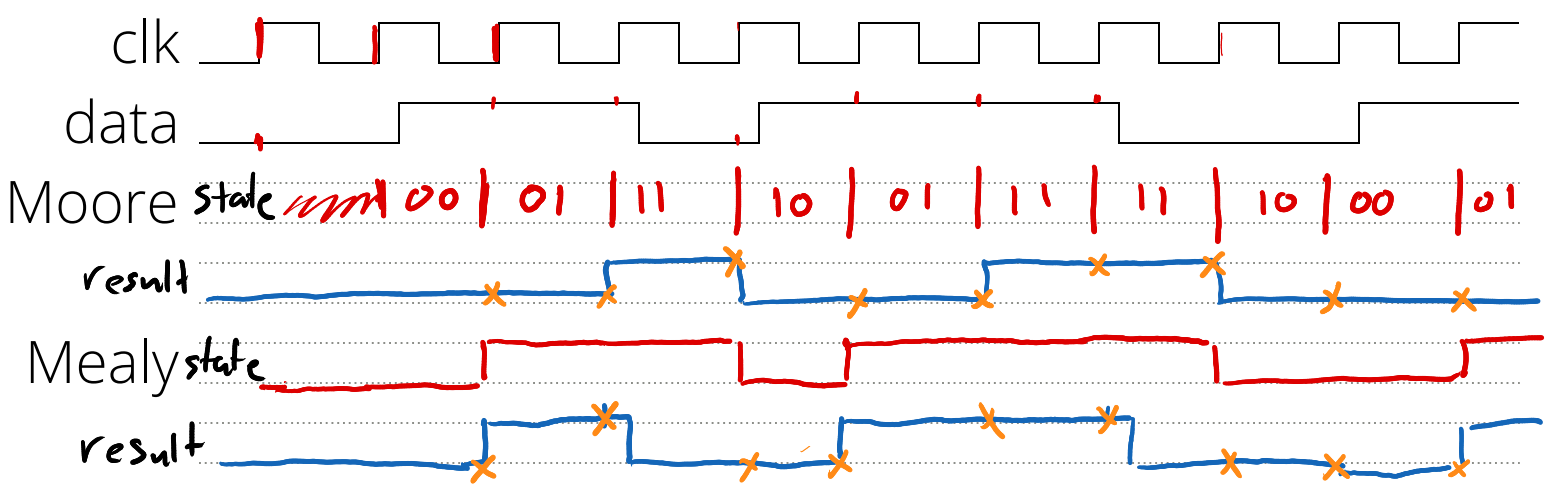
  Review materials up after class!

- Paper HW 2 is due Thursday, solutions are online

Mealy vs Moore (See also Harris example 3.7)







When is this read by a downstream FF?

FSMs in SystemVerilog

Design a circuit which sets a flag high when the "data" input has been high for 3 clock cycles. The flag should stay high until the reset signal is asserted (i.e., = 1)