Part 1: How is memory structured?

Part 1: How is memory structured?

- **Wordline** activates a row (word) of the memory for reading/writing
- **Bitline** connects to a column, and reads/writes an individual bit
- Address specifies which word of memory to operate on
- **Decoder** takes the address (as a binary number) and turns on the corresponding wordline
- Data bus aggregates the bitlines to carry the complete word

Part 1: How is memory structured?



Reading / writing a word



An abstracted view of (read-only) memory

FPGA has 30 4096-bit memories



An abstracted view of (read-write) memory



Part 2: Inside SRAM and DRAM

SRAM is "**static** random-access-memory"

DRAM is "**dynamic** random-access-memory"

Inside SRAM

wordline enables transistors
bitlines override inverters and force a new value
wordline goes low again



Inside DRAM



Part 3: Why do we need different kinds of memory?

Memory (DRAM) vs CPU speeds



DRAM cell



DRAM cross section



(image from chipworks http://chipworksrealchips.blogspot.com/2014/02/intels-e-dram-shows-up-in-wild.html)

Comparing memory technologies SRAM Hard drive Register file Cache DRAM Flash Spinning disk \$ \$ 2 \$\$ \$\$\$ \$\$\$\$ Cost/bit 10 ms + clms 1 cycle LIO cycles Speed >100 Non-volatile 1MB - 8MB 8GB - 32GB Typical size 64 bist x 32 req ITB+

Tape drives?!



Memory in the FPGA

Just like a flip-flop: describe the behavior you want, and Radiant will "infer" the RAM/ROM for you.

For next time

- 1. Continue with lab 6
- 2. Look for CATME survey