EE 201: Sequential logic timing

Steven Bell

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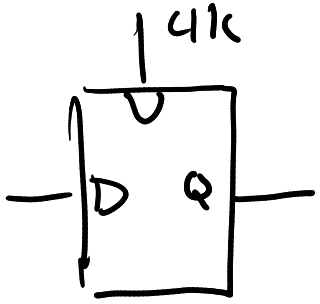
Tufts UNIVERSITY


Introduction to Digital Logic
Computer Programming
Verilog
VHDL
Fields of Enlightenment
Memory
Sequential Logic
Process Block Perils
YOU ARE HERE
Swamps of Arcane Syntax
State Machines
Flip-flop Pass
Computer Architecture
Plains of Combinational Logic
Desert of "How things used to be done"

By the end of class today, you should be able to

- Define **setup time** and **hold time**,
  and annotate them on a timing diagram
- Take a sequential circuit and a table of gate/FF delays, and **draw a timing diagram**.
- Calculate the **maximum frequency** a circuit can run at
- Calculate whether a circuit will have a **hold time violation**
- Optimize sequential circuits for speed, using spatial and temporal parallelism
- Explain what **metastability** is, and how to reduce it

Terms



- **Clock-to-Q propagation delay** (t_{pcq})

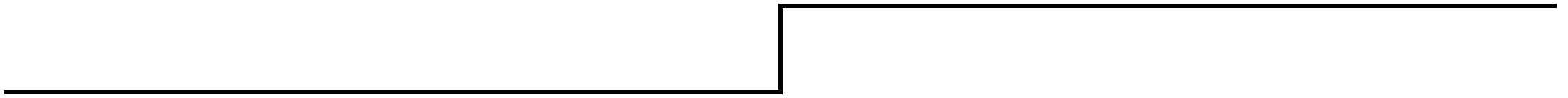
  Propagation delay from rising edge of clock to new value at Q

- **Setup time**

  Time before clock edge that FF needs to set up;
  input must be stable at least this much **before** clock edge.

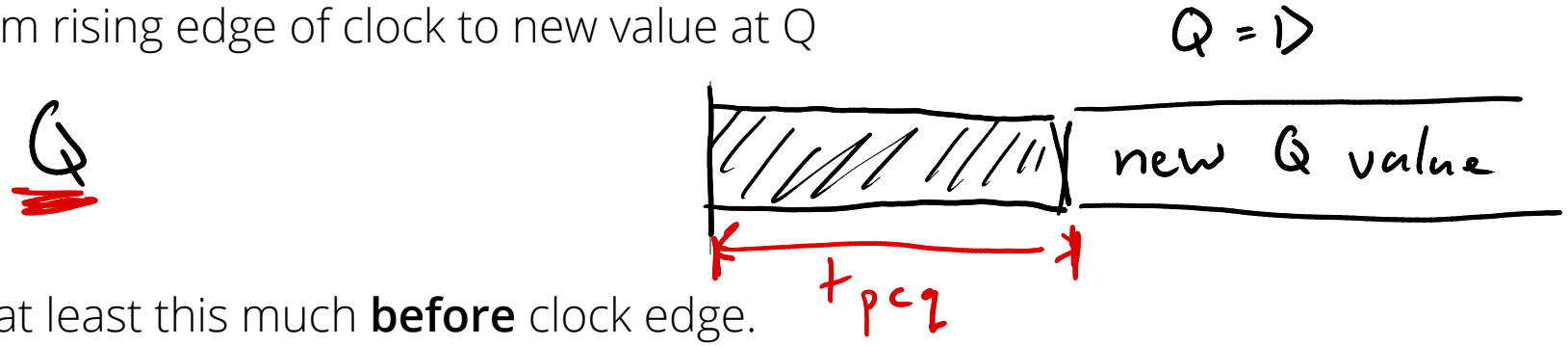
- **Hold time**

  Time after clock edge that FF needs value to hold still;
  input must be stable at least this much **after** clock edge.



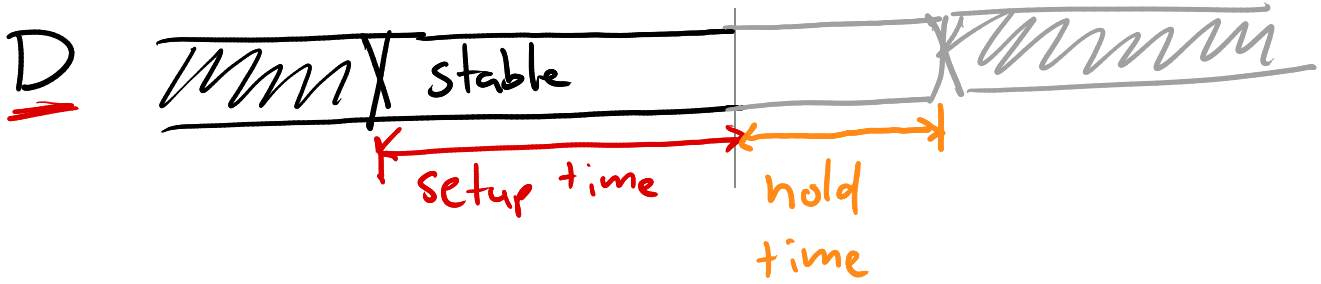
Clock-to-Q propagation delay (t_{pcq})

Propagation delay from rising edge of clock to new value at Q



Setup time

Input must be stable at least this much **before** clock edge.



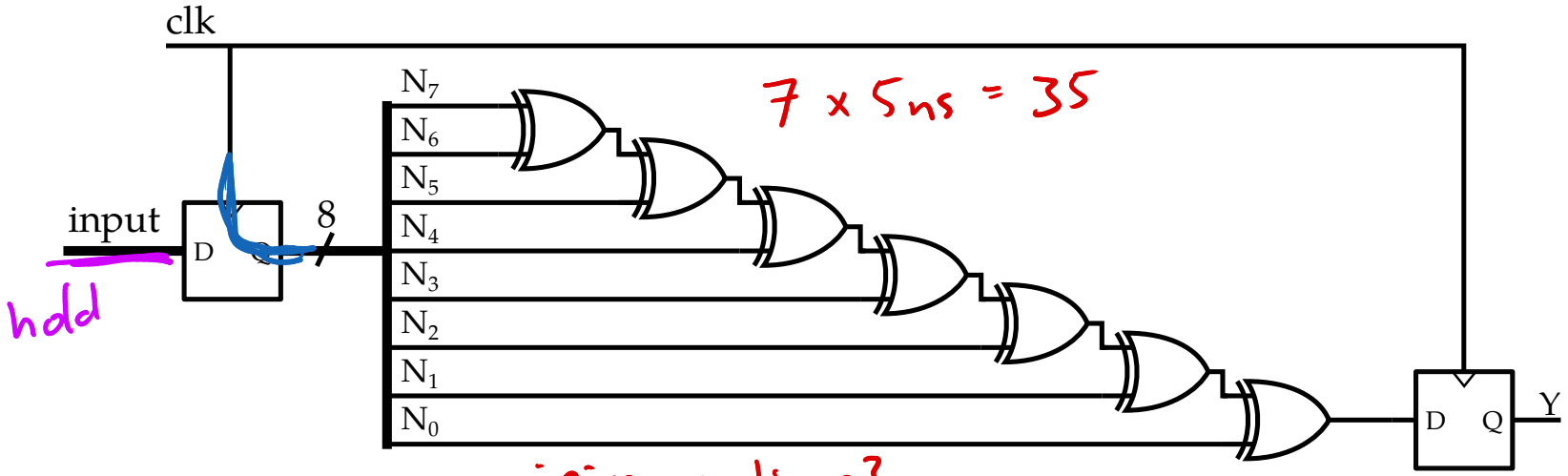
Hold time

Input must be stable at least this much **after** clock edge.

How fast can this run?

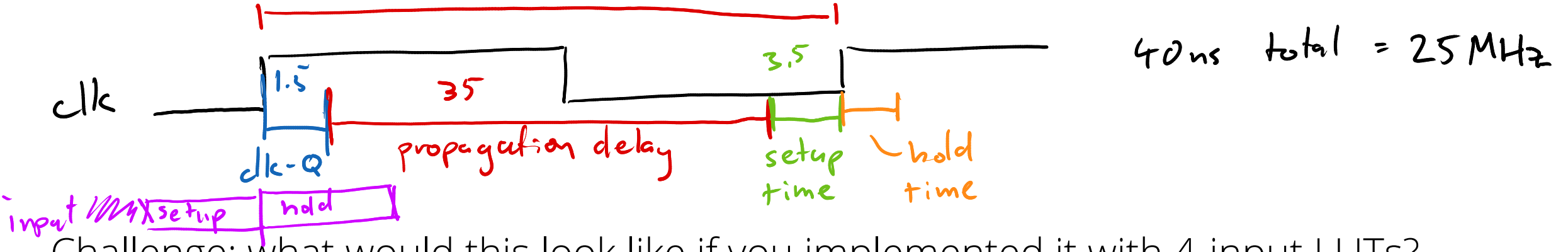
Don't we care about time to result?

(i.e., what is the maximum clock frequency before timing failure?)



Gate	t_{pd} (ns)	t_{cd} (ns)
2-input XOR	5.0	1.7
clk-Q	1.5	0.75
DFF setup time	3.5 ns	
DFF hold time	2.0 ns	

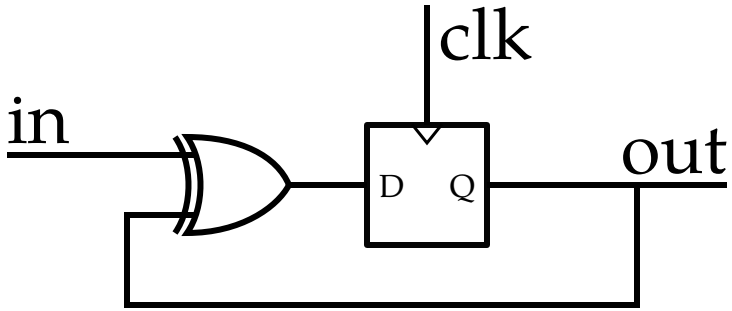
book value?



40ns total = 25MHz

Challenge: what would this look like if you implemented it with 4-input LUTs? How fast would it run?

How fast can this run?



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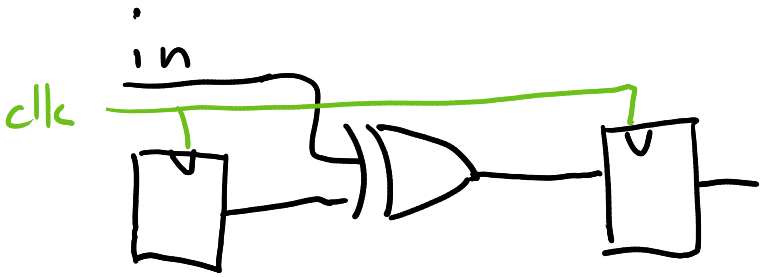
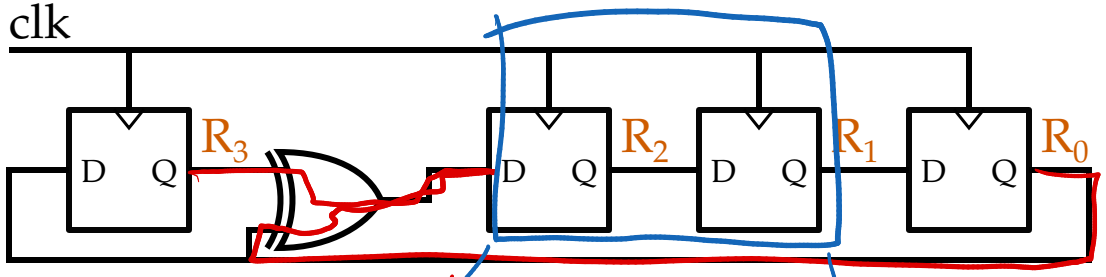


clk-q + XOR + setup

1.5 5 3.5 = 10ns = 100 MHz

Can this run at 75 MHz?

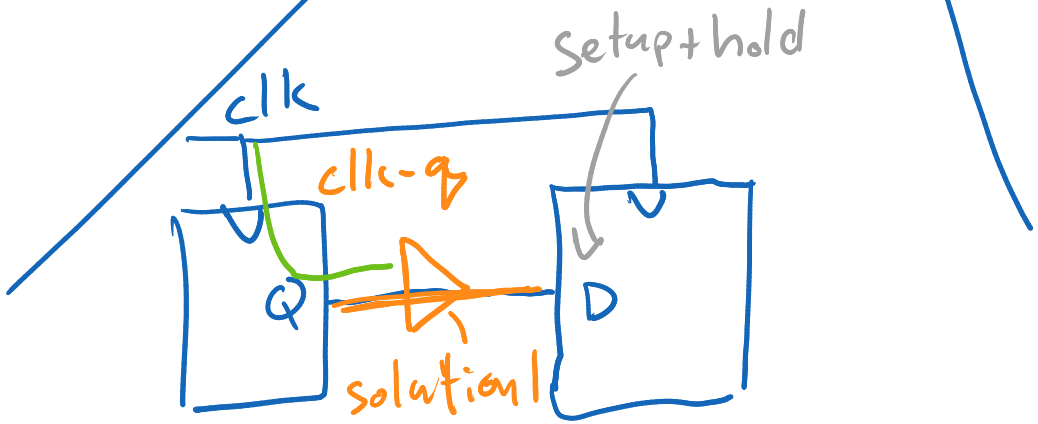


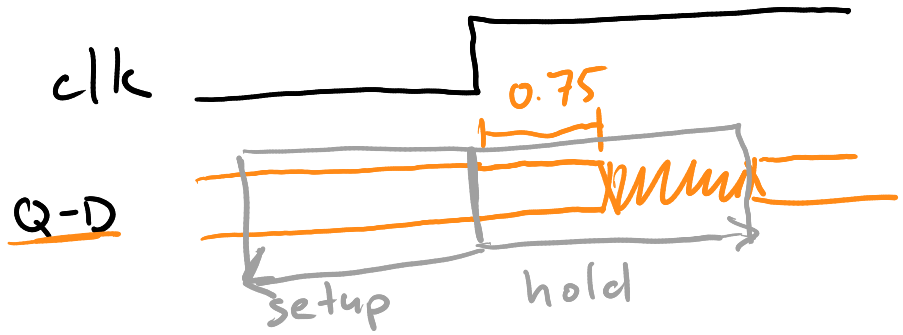
critical path → 100 MHz (prev. slide)

Gate	t_{pd} (ns)	t_{cd} (ns)
2-input XOR	5.0	1.7
clk-Q	1.5	0.75

DFF setup time 3.5 ns
DFF hold time ~~2.0 ns~~ < 0.75 ns

Real solution!





t_{cd} = 0.75 ns but hold time is 2 ns

Those equations look pretty complicated; do we have to memorize them?

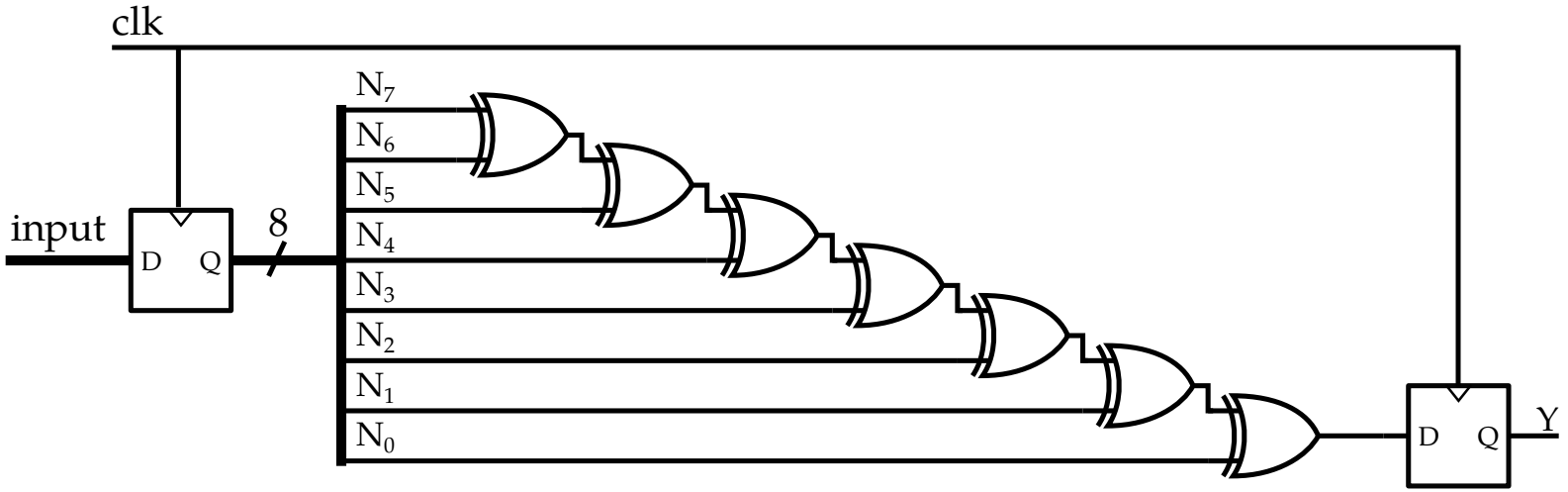
Those equations look pretty complicated;
do we have to memorize them?

Please don't.

You'll make your head hurt,
do poorly on the exam,
and forget all of it two months from now.

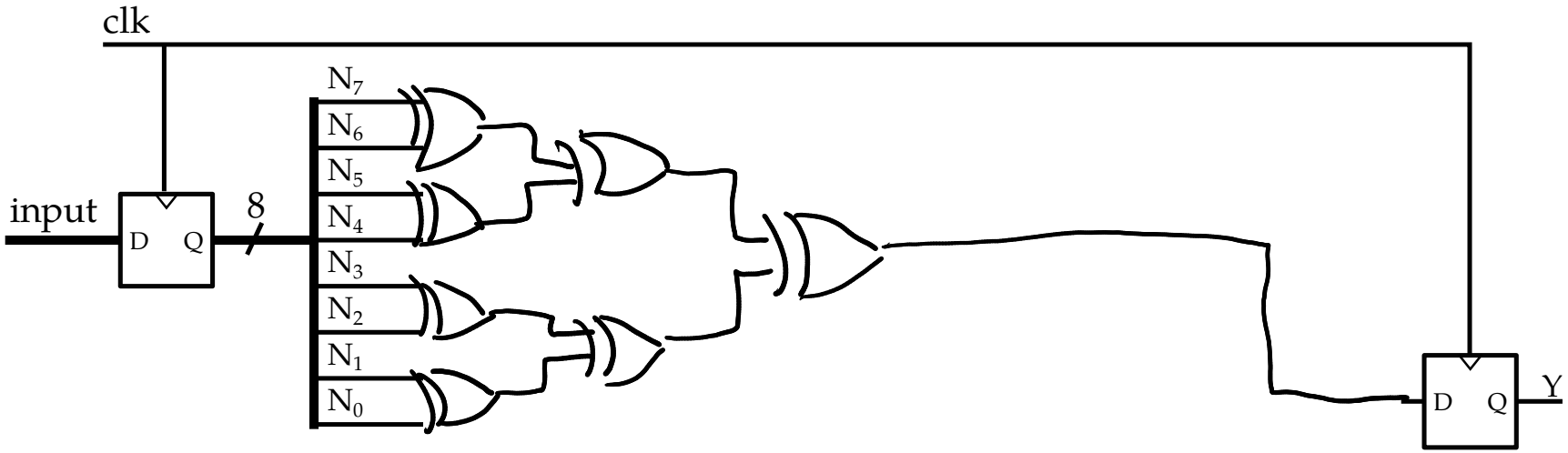
How do we speed this up?

25 MHz



Speeding up the XOR circuit

1.5 + 3 XOR × 5 = 15 + 3.5 = 20 ns = 50 MHz



Other ways to speed up the circuit?

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Metastability

What happens if a flip-flop input (D) isn't a stable low or high value?

The digital abstraction is broken!

But how would that happen?

1) An external input is giving your circuit a non-digital voltage

2) There is a setup time violation

3) You have a digital input from an external source

4) You have more than one clock in your design

But how would that happen?

1) An external input is giving your circuit a non-digital voltage

    Don't do that, silly!

2) There is a setup time violation

    Run slower / fix your design to meet timing

3) You have a digital input from an external source

    Use a synchronizer

4) You have more than one clock in your design

Does metastability actually matter to me?

Yes, you may see it on your FPGA!

Metastability in practice: inside an Arduino pin

Figure 13-2. General Digital I/O(1)