

# Warmup

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# EE 201: RISC-V assembly

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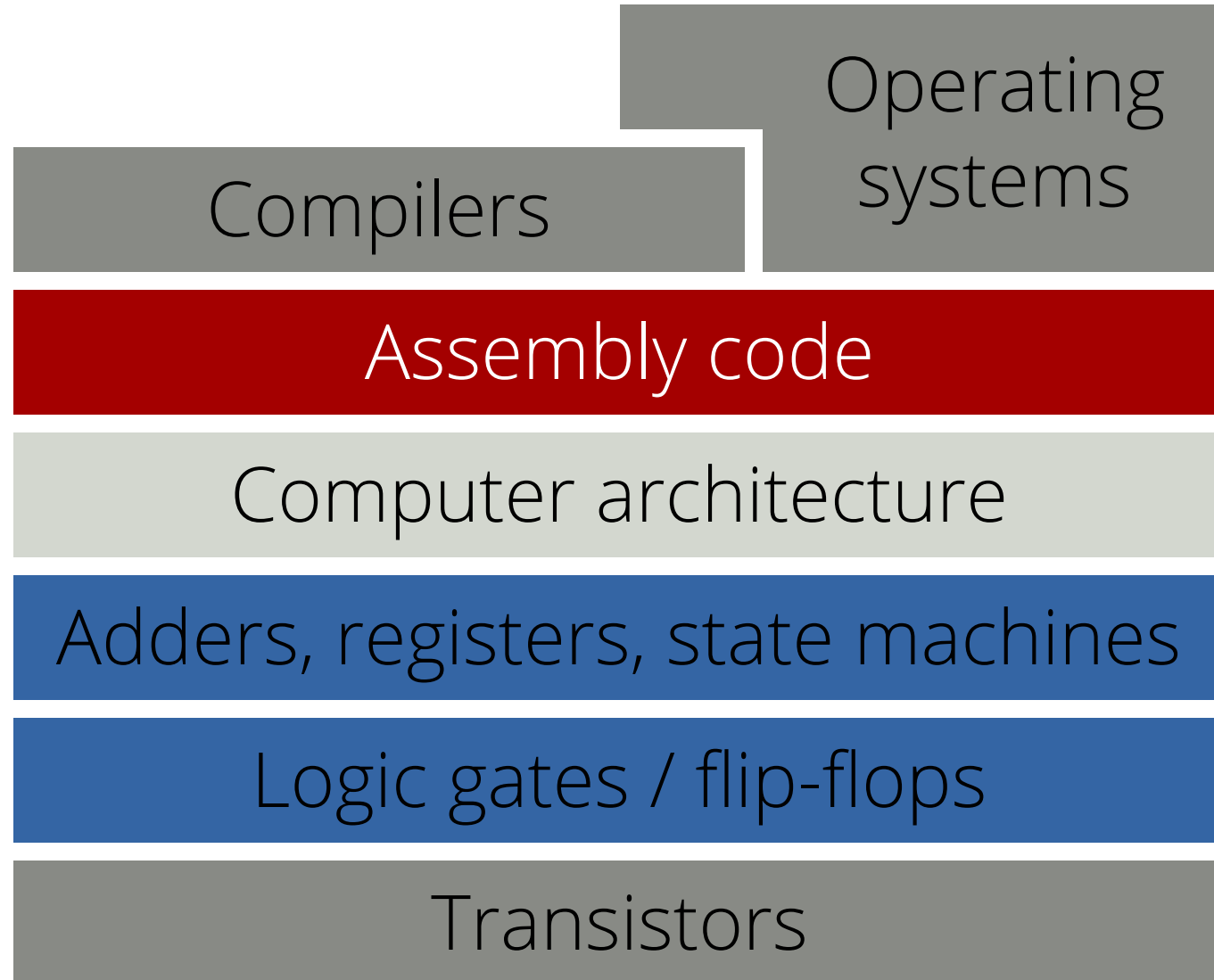
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# By the end of class today, you should be able to:

- Explain what an instruction set architecture (ISA) is
- Describe the registers available on a RISC-V processor
- Write RISC-V (RV32I) assembly code to do basic math
- Use branch instructions to implement if-else/loops/etc

We'll talk about memory and functions on Thursday!

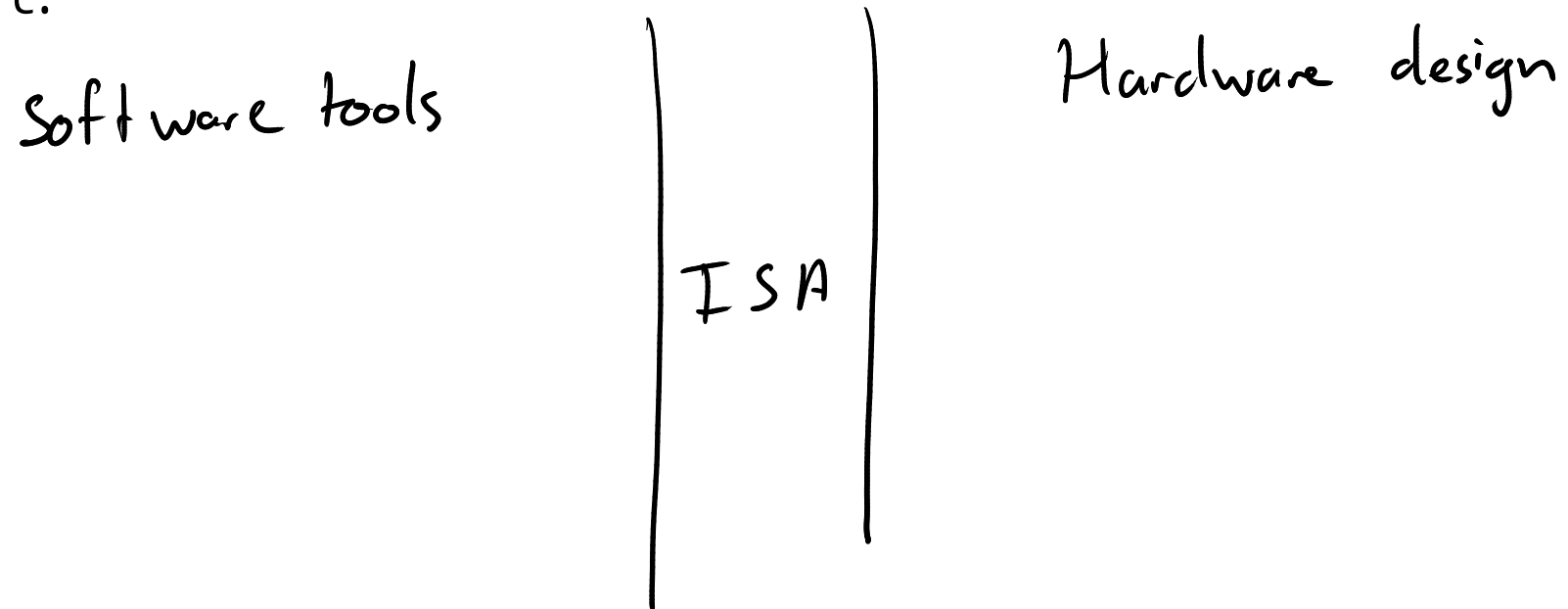
# The big picture



# What's an architecture?

"The programmer's view of the computer."

The contract between hardware and software: the set of things the software can ask the hardware to do, and what happens as a result.



# Intel x86: a success/horror story

A modern processor can run code from ~40 years ago

A modern processor has to support code from ~40 years ago!

# RISC-V

Pronounced "risk five"

A relatively new ISA developed at Berkeley

Follows reduced instruction-set computing (RISC) principles

- Support a small number of simple instructions

Defined as a base instruction set with optional extensions

- We'll be using RV32I, which is the 32-bit version with no extensions

# Why RISC-V in this course?

It's a real ISA, growing in commercial adoption

We can use a normal C compiler (gcc/clang) to write code for it

Simple enough to understand in one semester

A summary of all of RV32I fits on one page



# RISC-V general-purpose registers

RV32I defines 32 general purpose registers, **x0** through **x31**

**x0** is special: it is always 0

All other registers work the same, but by convention some are used for specific things (e.g., function arguments)

# Let's write some code!

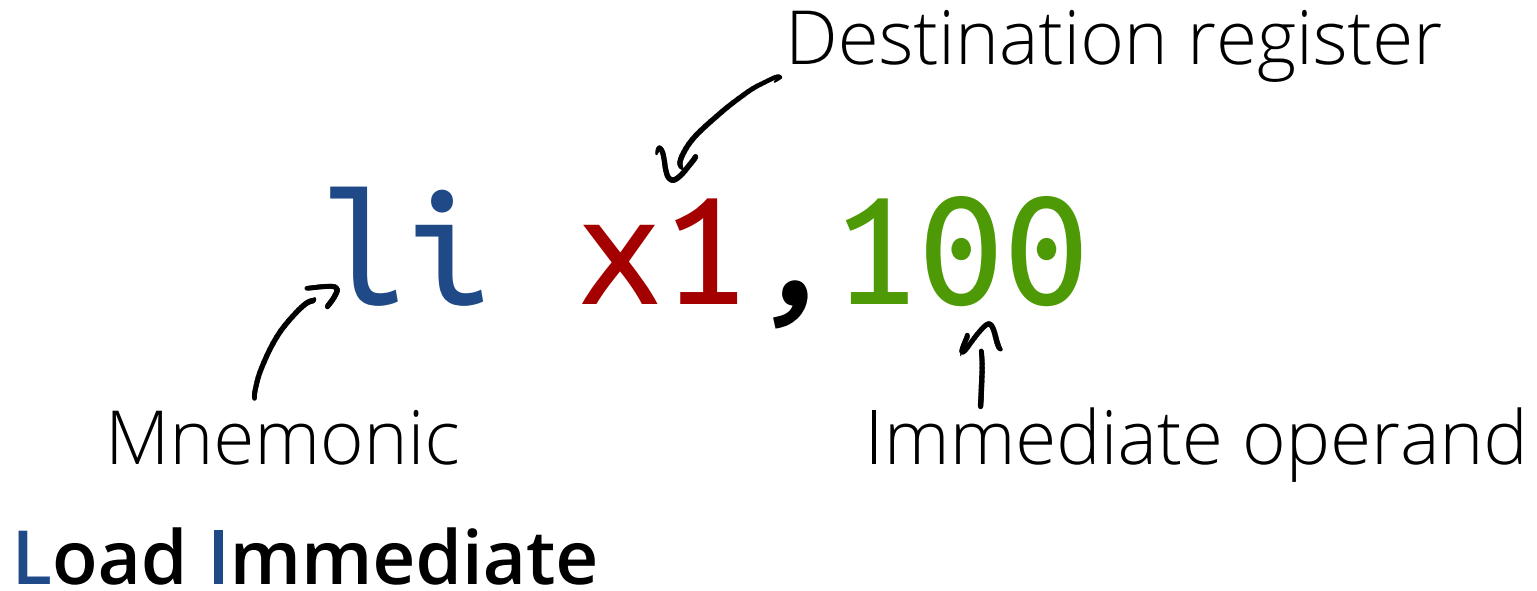
li x1, 100

Mnemonic

Destination register

Immediate operand

**Load Immediate**

The diagram shows the assembly instruction 'li x1, 100'. The 'li' is in blue, 'x1' is in red, and '100' is in green. An arrow points from the text 'Mnemonic' to 'li'. Another arrow points from 'Destination register' to 'x1'. A third arrow points from 'Immediate operand' to '100'. Below the instruction, the text 'Load Immediate' is written in blue.

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# Pseudo-instructions??

`addi x1, x0, 1`

$$x1 = x0 + 1$$

↑  
zero!

OPERATION dst, src1, src2

ADD src1 + src2 2 registers

SUB src1 - src2

SLL shift left

SRL) logical right

SRA arithmetic

SLT src1 < src2

SLTU 1111 < 0110?

OR logical OR

AND " AND

XOR " XOR

2 shift by 1 4  
0010 → 0100  
2 0010 → 0001  
-8 -4  
1000 → 1100  
"sign-extend"

OPERATION dst, src1, immediate  
reg + value

ADDI

No SUBI! use negative immediate

SLLI

SRLI

SRAI

SLTI

SLTIU

ORI

ANDI

XORI

# Practice time!

Write an assembly program which calculates

$$100 + 100 + 5$$

Try some of the other operators!

# How do I make choices?

Use a branch!

$B = Q$  branch if equal

# Practice time

Write a program that computes the absolute value of the value stored in **x1**. (Use li to load various values to test it!)

# Loops

A while loop has the form:

TOP

check if condition is false, and branch to BOTTOM if so

[ body of loop ]

unconditionally branch back to TOP

BOTTOM



# Practice time

Write a program that computes the sum of the natural numbers from 0 to 10.

if ( m ) {

} else {

}

Bm else

stuff if true

BEQ x0,x0, bottom

else:

stuff if false

...

bottom:

...

while ( ~ ) {

top:  
B ~ bottom (check condition)  
loop stuff...

BEQ x0, x0, top

bottom

}