Name: _____

ES 4 Exam 2 practice problems

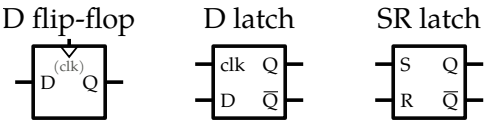
Fall 2024

Part 1: Sequential building blocks and VHDL

(a) For each of the VHDL code snippets below, draw the circuit that will be created. Each snippet is an architecture for the following entity:

```
entity widget is
  port(
    clk : in std_logic;
    a : in std_logic;
    b : in std_logic;
    result : out std_logic);
end;
```

The schematic elements for latches and D flop-flops are shown below for reference.



(a)
```
architecture first of widget is
begin
  process(clk)
    if rising_edge(clk) then
      result <= a and b;
    end if;
  end process;
end;
```

(b)
```
architecture second of widget is
begin
  process(clk, a, b)
      result <= a and b;
  end process;
end;
```

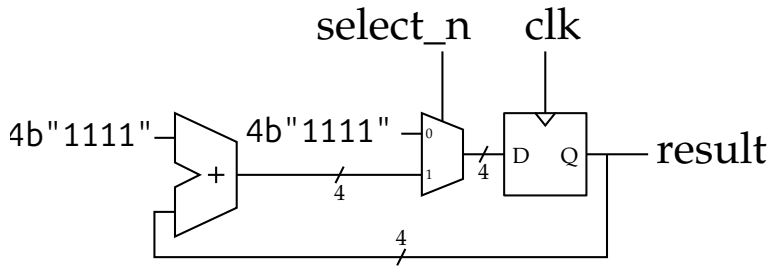
(c)
```
architecture third of widget is
begin
  process(clk, a, b)
    if(clk = '1') then
      result <= a and b;
    end if;
  end process;
end;
```

(d)
```
architecture fourth of widget is
  signal a_tmp : std_logic;
begin
  process(clk)
    if rising_edge(clk) then
      a_tmp <= a;
      result <= a_tmp and b;
    end if;
  end process;
end;
```

(e)
```
architecture fifth of widget is
  signal a_tmp : std_logic;
begin
  process(clk)
    if rising_edge(clk) then
      result <= a_tmp and b;
    end if;
  end process;
  a_tmp <= a;
end;
```

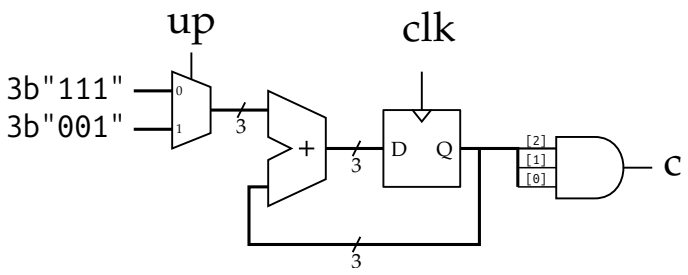
Part 2: Writing VHDL

Write VHDL code to create the circuit below. The entity has been started for you.




```
entity countdown is
  port(
    clk : in std_logic;
    select_n : in std_logic;
    result : out unsigned(3 downto 0));
end;

architecture synth of countdown is
begin
```

Write VHDL code to create the circuit below. The entity has been started for you.



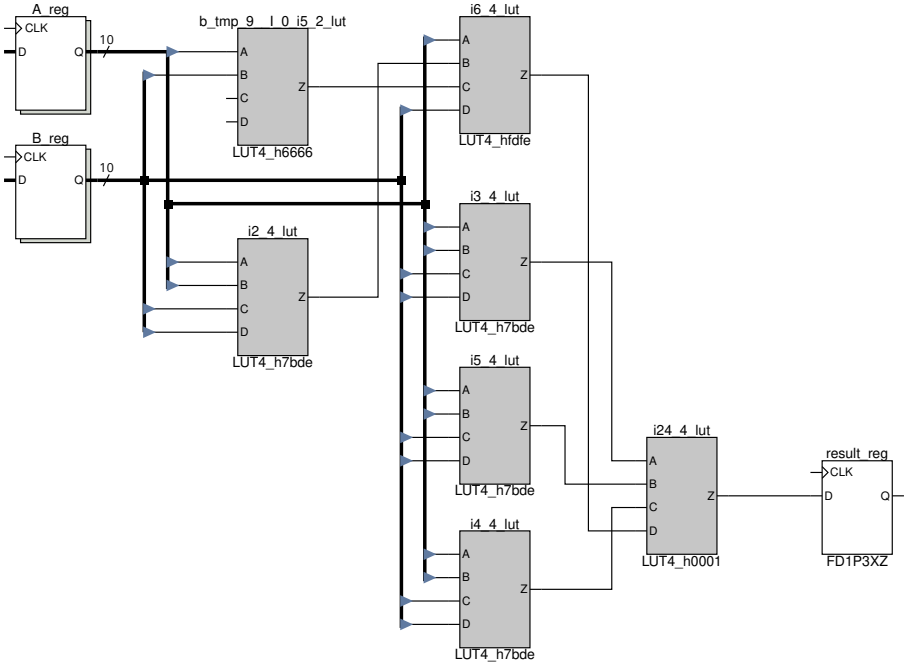

```
entity updown is
  port(
    clk : in std_logic;
    up : in std_logic;
    c : out std_logic;
end;

architecture synth of updown is
begin
```

Part 3: Timing

The iCE40UP5K FPGA has the following timing characteristics[1]:

Flip-flop clk-to-Q t_{pd}	1.0 ns
Flip-flop setup time	0.2 ns
Flip-flop hold time	0 ns
LUT input-to-output (A/B/C/D to Z) t_{pd}	0.5 ns

The circuit below is an actual FPGA implementation which checks whether two 10-bit signals (stored in `A_reg` and `B_reg`) are equal. The bold lines are the 10-bit signals, with individual bits going into the LUTs.



What is the maximum frequency this circuit could be clocked at?

[1] These numbers are taken from the Radiant P&R report and rounded for simplicity.

Part 4: Memory

A memory has 8-bit words and a 10-bit address bus. Assuming that all of the possible addresses are valid, how many bits does it store?

Sketch a block diagram for this memory, assuming that it is a single-ported RAM. That is, it can be both read and written, but it's not possible to read and write to different addresses at the same time.