ES 4 exam 2 study guide

The second exam will be comprehensive in that the material in the second half of the course builds on the material from the first half.

Latches and flip-flops

- Given a circuit containing a D latch or a D flip-flop, draw a timing diagram to illustrate how and when the output changes.
- Write VHDL code to create D latches and D flip-flops, and explain how the lines of VHDL work to describe a flip-flop or latch.
- Explain why we often prefer flip-flops over latches.

Basic sequential circuits

- Sketch the general structure of a sequential circuit.
- Draw a schematic for a binary counter, shift register, one-hot counter, and LFSR.
- Given a short snippet of VHDL code, draw the circuit that will be created
- Write VHDL code to describe counters, shift registers, and other sequential circuits (similar to the VHDLweb problems)

State machines

- Explain what a state machine is in terms someone just beginning this course could understand
- Explain the difference between a Mealy and Moore state machine
- Given an English description of a system, do the following for both Moore and Mealy implementations:
  - Draw the state diagram
  - Determine how many bits of state are necessary, and choose state encodings
  - Write truth tables and logic equations for the state transitions and outputs
  - Draw the complete logic circuit diagram for the FSM

Timing sequential logic

- Define setup time and hold time, and annotate them on a timing diagram
- Given a sequential circuit and a table of gate/flip-flop delays, draw a timing diagram and calculate the maximum frequency at which the circuit could run.
- Given a circuit, explain how temporal and spatial parallelism could be applied to increase the overall throughput.

Memory

- Describe how a memory is organized in terms of bits, bytes, words, addresses, etc.
- Sketch a block diagram for a RAM or ROM, showing the widths of the input and output ports as appropriate.