ES 4 ModelSim/Questasim tutorial

ModelSim is an HDL simulation tool widely used in industry. It was rebranded as "Questasim" a few years ago, but Mentor continues to distribute the older version under the ModelSim name. The software hasn't changed much, so we will use the names interchangably in this document.

1 Running ModelSim

1.1 Virtual machine image

Modelsim is installed on the ES 4 virtual machine image. Just click the "M" icon in the launcher.

1.2 Install locally

Mentor provides a free version of ModelSim which works for up to 10,000 lines of code. You can download it for Windows here: https://www.mentor.com/company/higher_ed/modelsim-student-edition

1.3 Use Halligan labs

Linux (Halligan labs 116, 118, 120)

- Open a terminal instance
- Type `use questasim` to set up the environment
- Type `questasim &` to run

1.4 Remote Access

- For a tutorial on setting up a remote connection to use ModelSim through SSH with PuTTy, see the steps at this link: http://www.geo.mtu.edu/geoschem/docs/putty_install.html
- Log into one of the Halligan cluster machines (e.g., `homework.eecs.tufts.edu`), and follow the directions above under "Use Halligan labs".

If the editor font is invisibly small on Linux, edit the file `~/.modelsim` (Questasim uses the same file) and put a - (dash / minus sign) in front of the font size for `textFontV2`, like so:

```
{textFontV2 {{Courier 10 Pitch} -14}}
```

2 Setting up the project

2.1 Create a new project

1. Close out of the "IMPORTANT Information/Jumpstart" pop-up window that appears when you open the program.
2. Select *File* → *New* → *Project*
3. Give your project a name, e.g. "ES4_Lab1"
   - This name should be one continuous word, but it does not have to be the same name as your entity/entities.

4. Select a location for the directory where all your project's files will live.
   - Note: We suggest making different folders for each lab.
5. Leave the rest of the settings intact and press OK.

2.2 Add/create files

- If you have not already written your VHDL, select "Create New File"
  - Provide the filename for the VHDL file you will write.
  - Warning: this file name must match the name of the entity it describes, i.e. "AND2.vhd" should have the entity statement "entity AND2 is . . . "
- If you have already written your VHDL, select "Add Existing File"
  - Find the file you wrote, and choose whether or not it you want it to be copied into the directory you chose earlier (where the rest of the project lives).
  - Note: If you would like all your project files in the same folder, we recommend copying the source into the project directory; any edits you make in ModelSim will then be saved in the version that lives in the project directory.

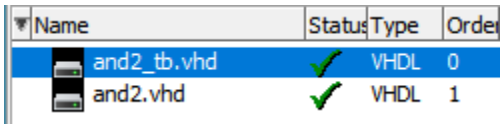
2.3 Notes

- If you accidentally switch or close out of a project you were in before, you can likely find it again in *File - Recent Projects*.
- You cannot have multiple filenames whose only difference in name is letter case, e.g. and2.vhd and AND2.vhd.

3 Running a Simulation

3.1 Compile

1. Compile your source file(s) by selecting *Compile* → *Compile All*, or by Shift-clicking/Ctrl-clicking the desired source(s) and using *Compile* → *Compile Selected*
2. Your failed compiles, if any, will show up in red in the Transcript window at the bottom of the screen.
   - Double-click any of these red lines to see the errors in each file.
3. Once your files are free of errors, you will see green check marks in the "Status" column:



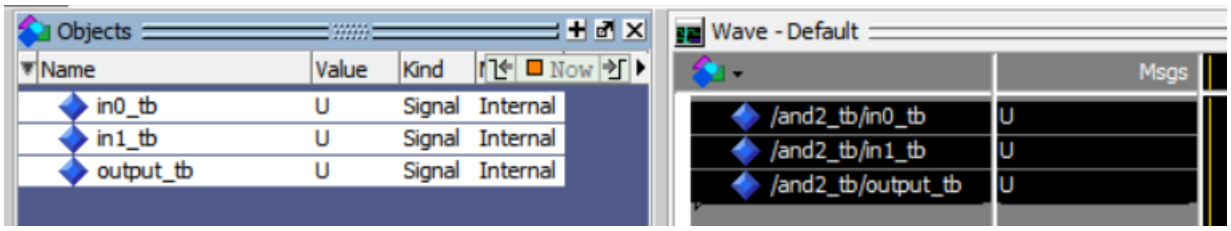
3.1.1 Common Errors

- Final Semicolon
  - A proper port description has semicolons at the end of each line, but the one on the final line of ports leaves the semicolon until after the closing parenthesis.
  - Note: Be sure to check surrounding lines of code near an error, because if it is related to a missing semicolon, the error line number may refer to the line *after*, which fails to compile.

- Matching Names
  - If you begin an **entity** statement with "entity AND2 is", it may end with the **entity** name, i.e. "end AND2", or just with "end".
  - If you begin an **architecture** statement with "architecture arch_1 of AND2 is", it must end with the **architecture** name, i.e. "end arch_1".

3.2 Configure Simulation

1. Select *Simulate - Start Simulation*
2. Click the + sign next to the "work" directory to expand it and view your entities
   - Note: "work" is the "working directory," a directory made by ModelSim where all your VHDL entities are compiled to.
3. Click on the name of the **testbench file** you want to simulate ("e.g. AND2_tb") and hit OK
4. Highlight all desired signals in the Objects window that appears
   - Click the first source and Shift-click the final one to grab all signals
   - Or ctrl-click to select individual signals
5. Right click the selection, and choose "Add Wave" (this may appear as *Add* → *To Wave* → *Selected Signals*). Your end result should be the signals you selected appearing in the Wave section,



3.3 Running the Simulation

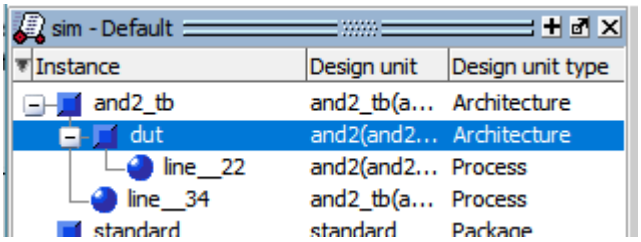
1. Choose a logical length of time for your simulation to run, and enter it in this text box **(with units!)**

2. Run the simulation using the Run button to the right of the time box:

3. At this point, you should evaluate both the waveform and text (assertion) of your circuit for performance, and if it works, call your TA over to confirm its functionality.
4. When you're finished, use *Simulate - End Simulation* to leave the simulation.

3.3.1 Navigating the Wave Window

- Click any point on the wave to move the cursor to it, and the values of each signal at that time will be shown in the "Msgs" column of the Wave Window. You can use these values to evaluate your waveform.
- Useful Keyboard Shortcuts:
  - I to Zoom In
  - O to Zoom Out
  - F to Zoom Fit (adjusts wave zoom to window size)
  - H to Hide the long prefix before each port name
- If it will grant you joy, you can change the color of various waveforms and their names by right-clicking on a signal and selecting Properties.
- You can add internal signals within the device under test by expanding the component in the "Instance" menu:



3.3.2 Debugging and Making Changes

- If you want to run your simulation for a different length of time, you can use the Restart button to the left of the time box:

- If your circuit does not work and you need to edit any source files, you do not have to leave the simulation completely!
  - Just make sure you re-compile your VHDL files and restart the simulation.