ES 4 Final project design

Submit a document describing the design of your final project. This must include:

- A block diagram of your FPGA logic, with the modules you plan to make in VHDL. Make sure to label all of the modules, the inputs/outputs, and the relevant bus widths.
- State diagrams for any state machines that you plan to use.
- Calculations for how much storage you will use. (e.g., a 16 x 16 pixel ROM with 6 bits/pixel will require 1536 bits of ROM; a 2-second mono sound clip at 8000 samples/second, 8 bits/sample will use 128kbits) Remember that you have a total of 120kbits of ROM on the FPGA.
- Little or no additional text.

This document does not need to be self-explanatory; its purpose is to 1) help you to think like an engineer as you work through the details of the design, and 2) help facilitate a discussion with your project mentor TA.

Submit your document on Gradescope; please use the group submission feature since that makes it much easier for us to give feedback to the whole team.