ES 4 ARMv7 assembly reference sheet

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Data-processing operations

For these operations, Src2 may be either an 8-bit immediate (if I=1) or the 4-bit ID of a register (I=0).

Operation	cmd	Assembly	Behavior
Bitwise AND	0000	`AND Rd, Rn, Src2`	Rd ← Rn & Src2
Bitwise OR	1100	`ORR Rd, Rn, Src2`	Rd ← Rn | Src2
Add	0100	`ADD Rd, Rn, Src2`	Rd ← Rn + Src2
Subtract	0010	`SUB Rd, Rn, Src2`	Rd ← Rn - Src2
Reverse subtract	0011	`RSB Rd, Rn, Src2`	Rd ← Src2 - Rn
Move	1101	`MOV Rd, Src2`	Rd ← Src2

If the S bit it set, the CPSR should be filled with the ALU result flags.

Memory operations

Operation	L	Assembly	Behavior
Store	0	`STR Rd , [ Rn ]`	Mem [Rn] ← Rd
		`STR Rd , [ Rn, #imm12 ]`	Mem [Rn + imm12] ← Rd
Load	1	`LDR Rd , [ Rn ]`	Rd ← Mem [Rn]
		`LDR Rd , [ Rn, #imm12 ]`	Rd ← Mem [Rn + imm12]

Branch

Operation	Assembly	Behavior
Branch	`B LABEL`	PC ← (PC + 8) + (imm24 << 2)

Conditional execution (Harris table 6.3)

	Name	cond	CPSR		Name	cond	CPSR
EQ	Equal	0000	Z	NE	Not equal	0001	$\overline{Z}$
HS	Unsigned higher / same	0010	C	LO	Unsigned lower	0011	$\overline{C}$
MI	Minus	0100	N	PL	Plus (positive or zero)	0101	$\overline{N}$
VS	Overflow set	0110	V	VC	Overflow clear	0111	$\overline{V}$
HI	Unsigned higher	1000	$\overline{Z}C$	LS	Unsigned lower or same	1001	$Z+\overline{C}$
GE	Signed greater / equal	1010	$\overline{N \oplus V}$	LT	Signed less than	1011	$N \oplus V$
GT	Signed greater than	1100	$\overline{Z}(\overline{N \oplus V})$	LE	Signed less / equal	1101	$Z+(N \oplus V)$
AL	Always	1110			(There is no "never")		