Warmup

Use a k-map to find a minimal implementation of this truth table:

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

$\bar{A}C + AD$

Respond at **pollev.com/stevenbell**

ES 4: Multiplexers and FPGAs

Steven Bell

20 September 2022

Tufts UNIVERSITY

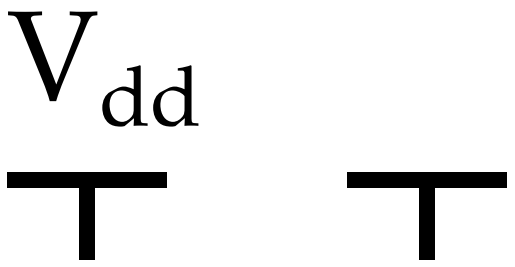
Logistics

- I'm working on HW 1; it will be due at least a week after posted
- You're invited for Thanksgiving

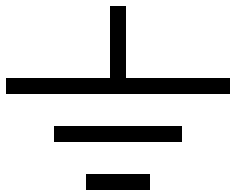
By the end of class today, you should be able to:

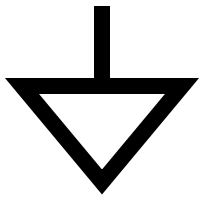
- Explain what a multiplexer is
- Draw a logic diagram using a 2^N-input multiplexer to implement an N-variable or (N+1)-variable boolean equation
- Describe the basic structure of an FPGA

Some schematic terminology



VDD 5V HIGH **1**

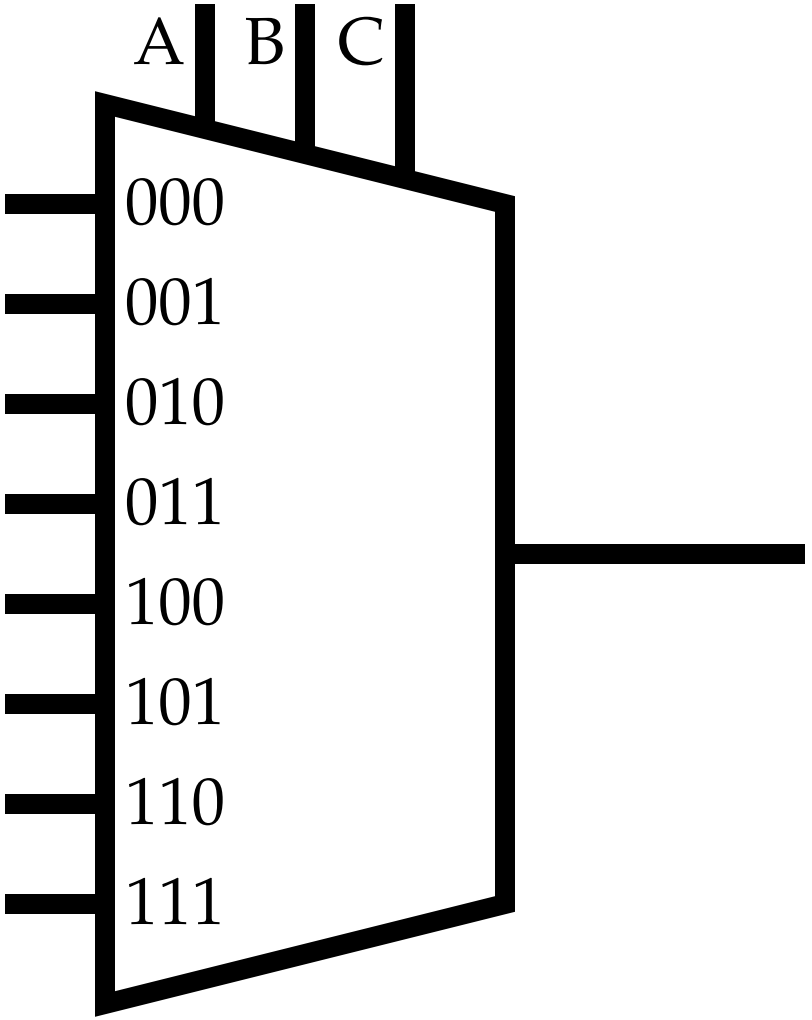




Ground 0V LOW **0**

Multiplexers

Select one of 2^N inputs based on the binary value of N control wires

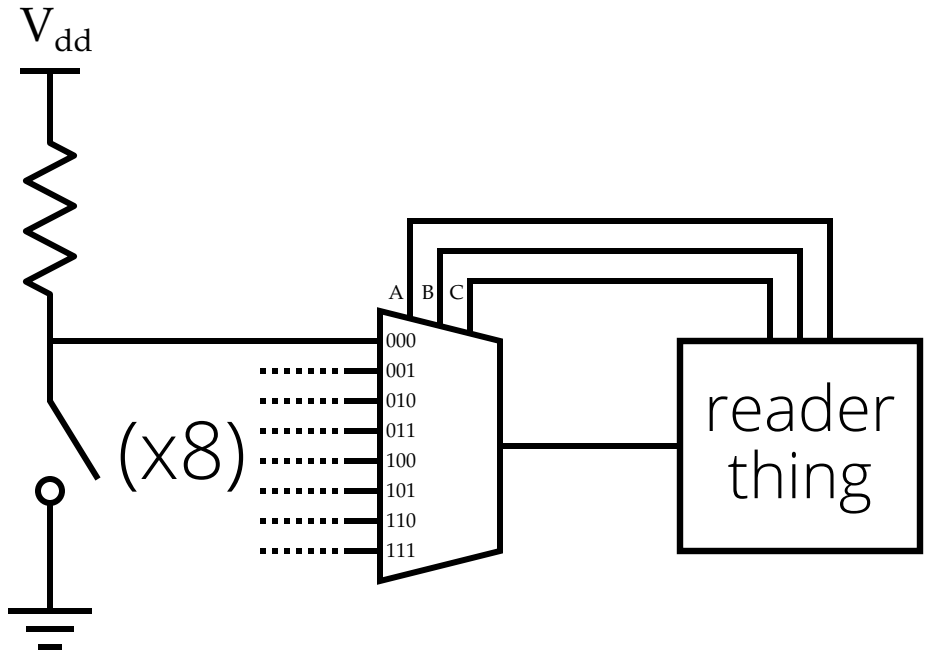


What good are multiplexers?

1) Allow you to select (or control) one signal out of many

A practical example

Suppose you want to read 8 switches
but you only have 4 inputs/outputs.

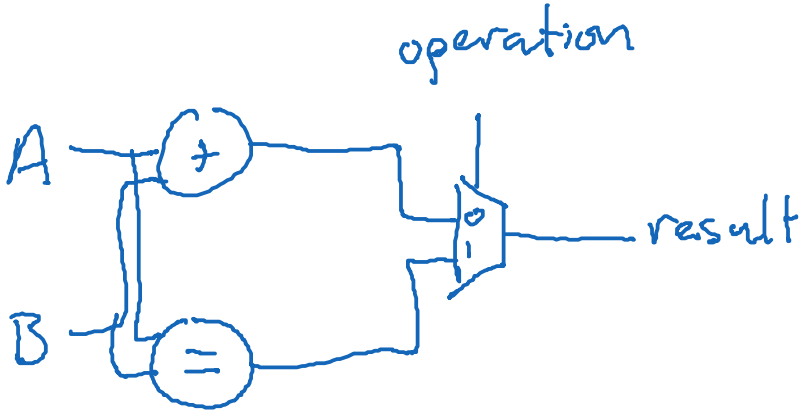


What good are multiplexers?

1) Allow you to select (or control) one signal out of many

1B) Allow you to make a choice based on a control value

It's like an **`if`** or **`case`** statement in software



What good are multiplexers?

1) Allow you to select (or control) one signal out of many

1B) Allow you to make a choice based on a control value

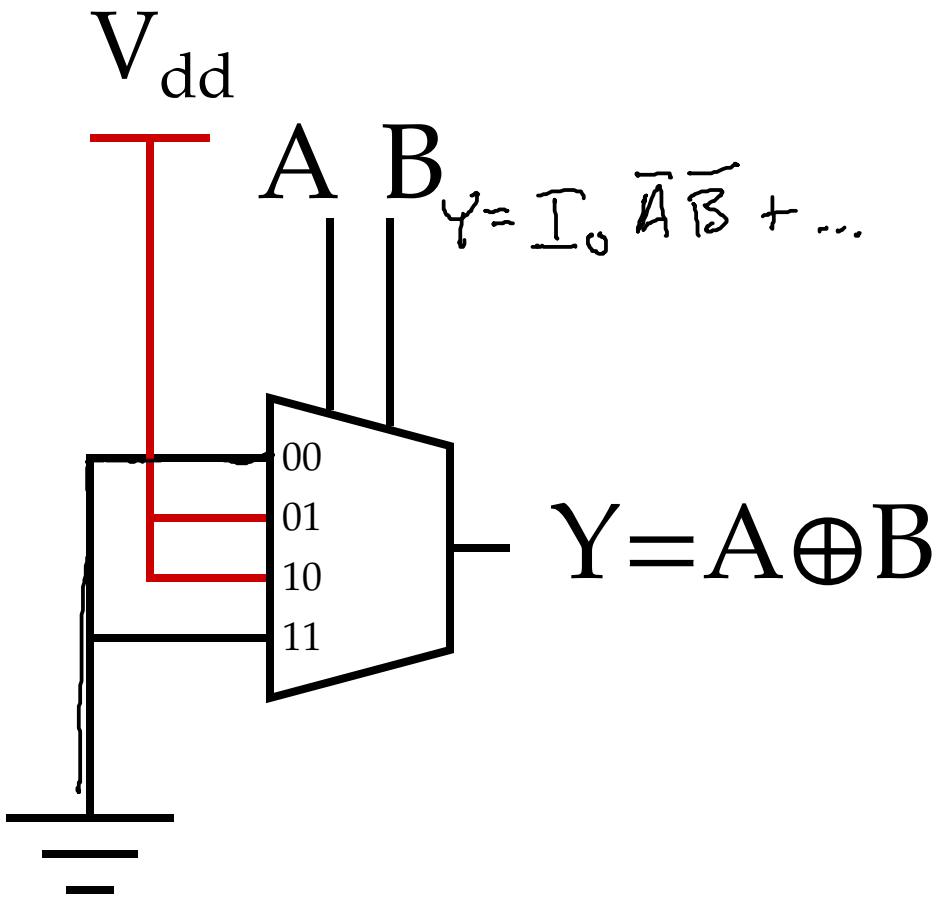
It's like an `if` or `case` statement in software

2) Make it easy to implement arbitrary logic functions

Implementing XOR

Using a mux as a look-up table (LUT)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

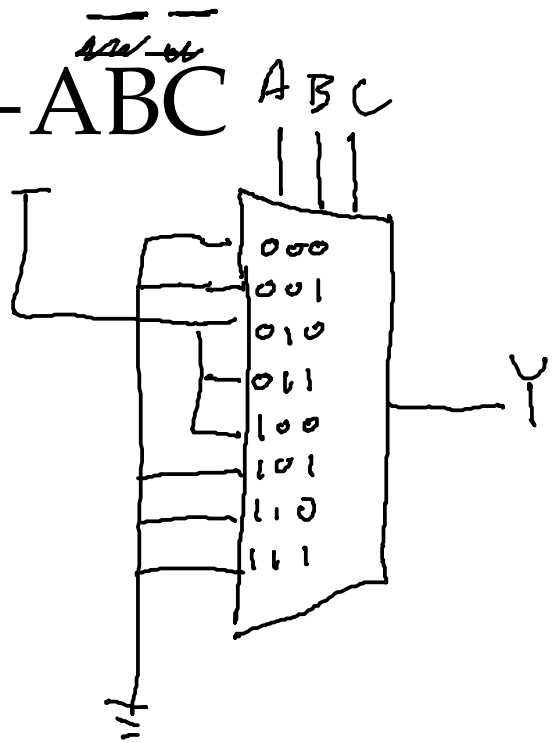


Multiplexer practice 1

Implement this logic equation using

1) 8:1 multiplexer
2) 4:1 multiplexer

$$Y=\overline{A}B+A\overline{B}C$$



A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Multiplexer practice 1

Implement this logic equation using

1) 8:1 multiplexer
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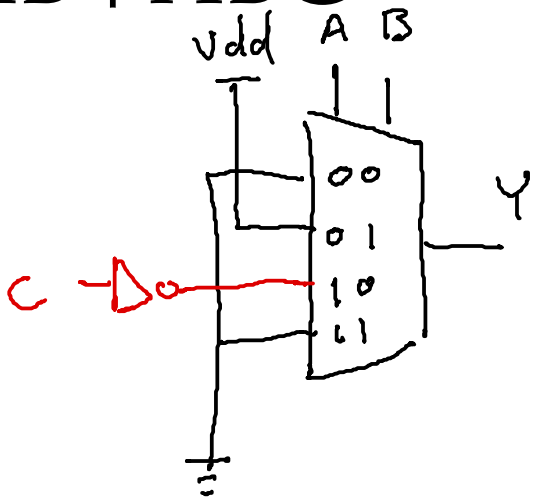
$$Y=\overline{A}B+A\overline{B}\overline{C}$$



A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Implement a 2-bit adder with multiplexers (Prelab 3)

How are you feeling about multiplexers?

Respond at **pollev.com/stevenbell**

Will a time come when it's cheaper to use a microprocessor than to implement something with discrete logic gates?

Respond at **pollev.com/stevenbell**

iCE40UP block diagram

Clock stuff

Fixed-function multipliers

Memory

Logic "fabric"

Fixed-function I/O modules

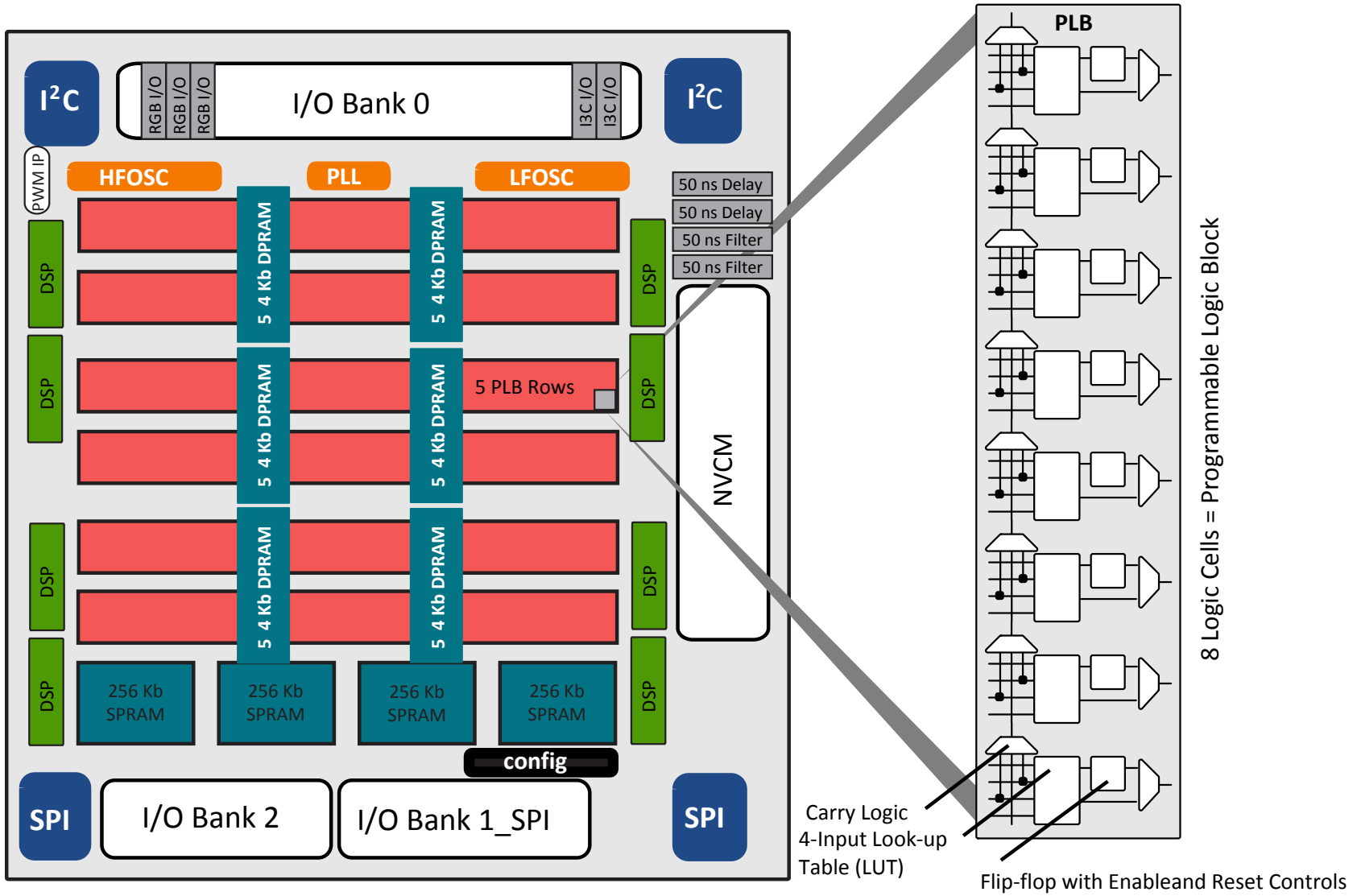


Figure 3.1. iCE40UP5K Device, Top View

iCE40UP logic element

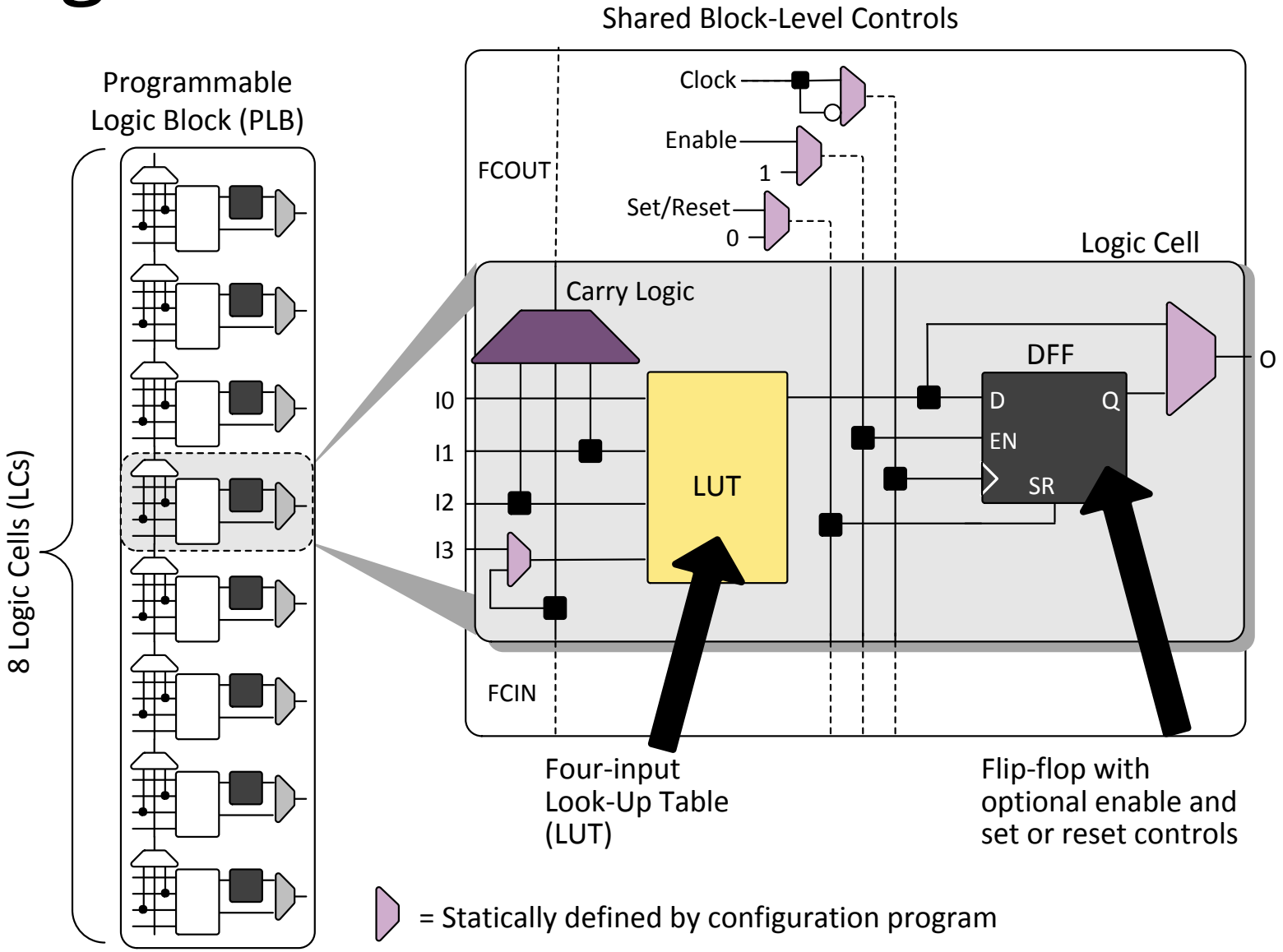
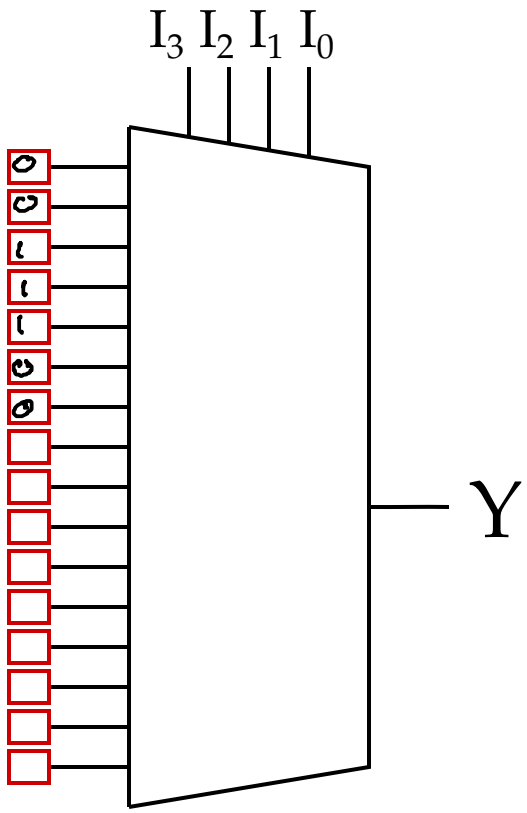


Figure 3.2. PLB Block Diagram

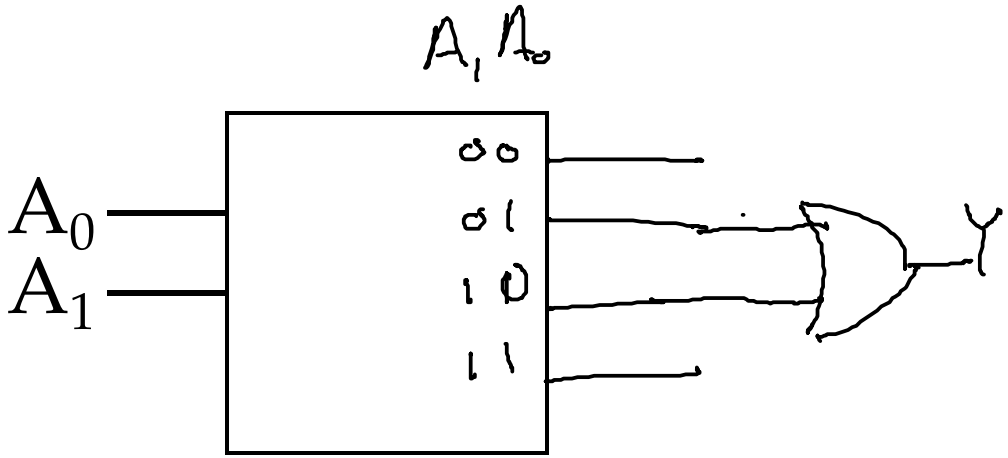
What's a LUT?

A look-up-table is basically a MUX where the inputs are statically configured to implement logic.



Decoders

Take a binary number as an input, and set the corresponding output high.



(An artifact found in the "desert of the way things used to be done")

What is one question you have after today's class?

Respond at **pollev.com/stevenbell**

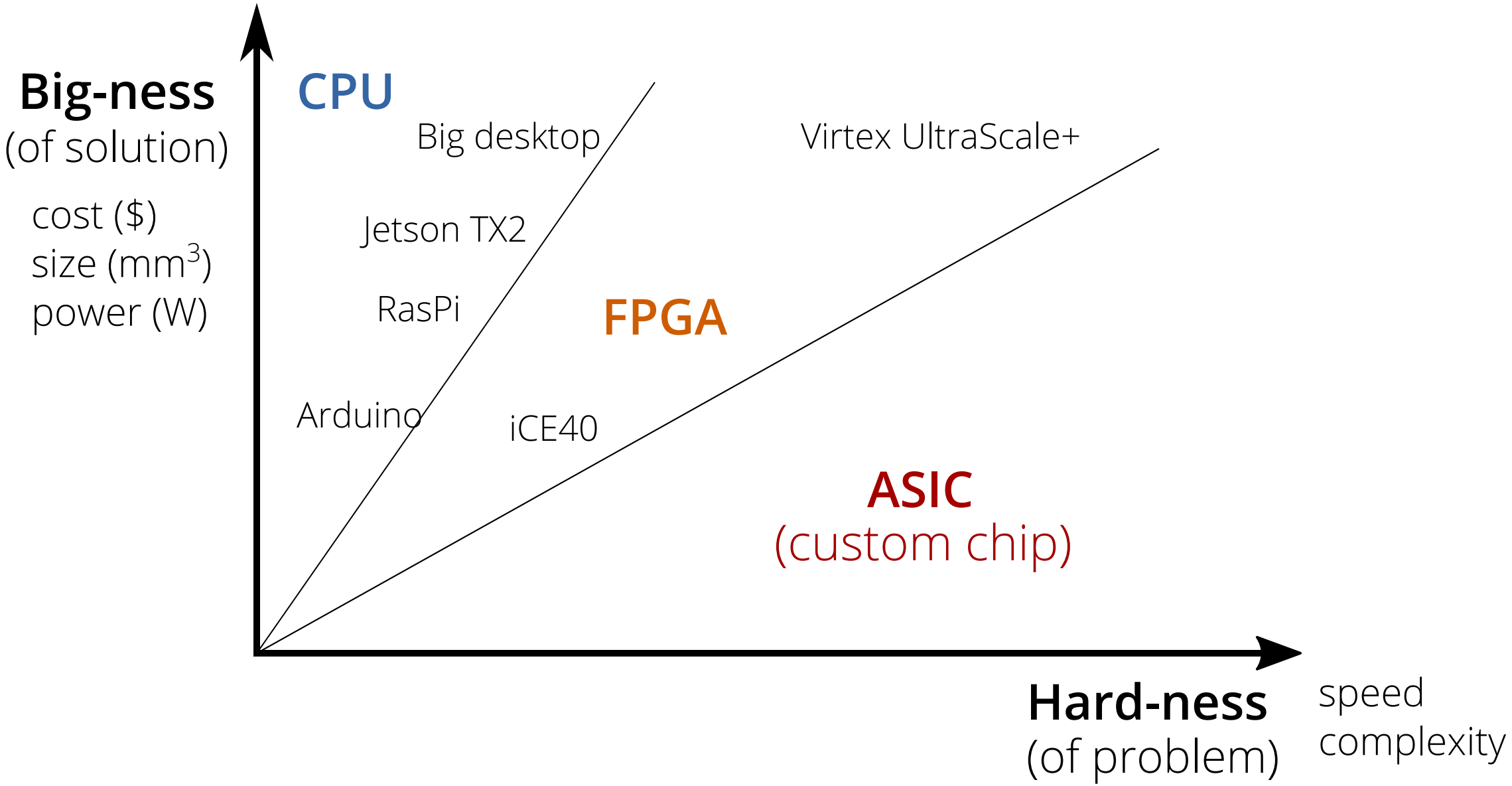
For Thursday

1. Read the book (2.9) and complete the reading check

2. Lab 2 report is due next week at your lab time

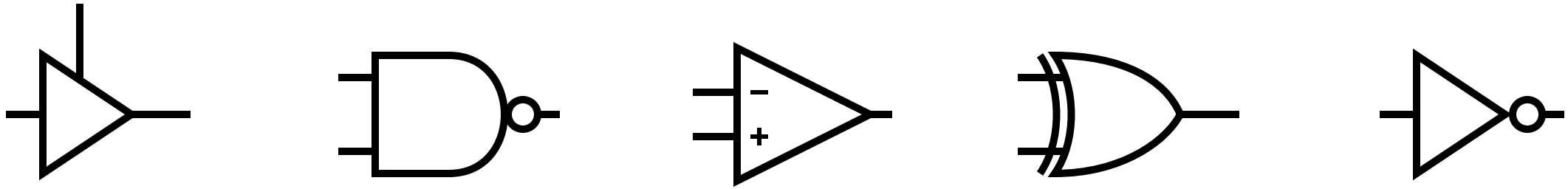
   See the video and handout on the course website

3. Prelab 3 is due next week 24 hours before your lab time


Big-ness
(of solution)
cost ($)
size (mm3)
power (W)
CPU
Big desktop
Jetson TX2
RasPi
Arduino
FPGA
iCE40
Virtex UltraScale+
ASIC
(custom chip)
Hard-ness
(of problem)
speed
complexity

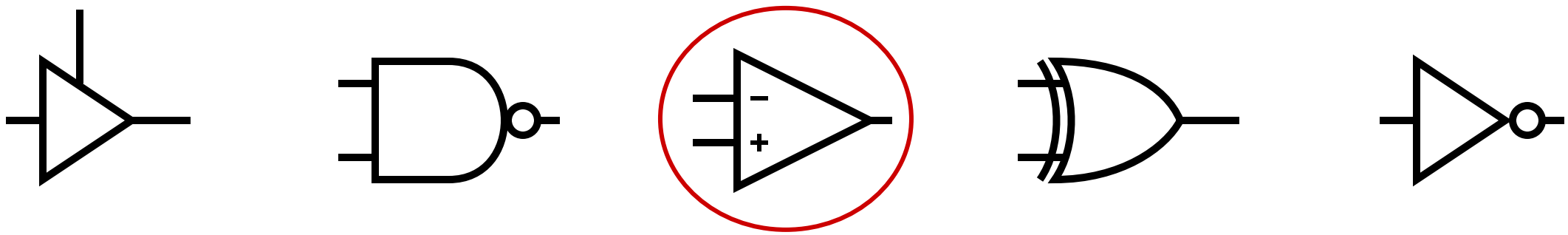
Terminology

Which of these is not a digital circuit element?



Terminology

Which of these is not a digital circuit element?



This is an op-amp!