Warmup

You are asked organize the **Boston Marathons**, which this year will be **five separate races** on the same course.

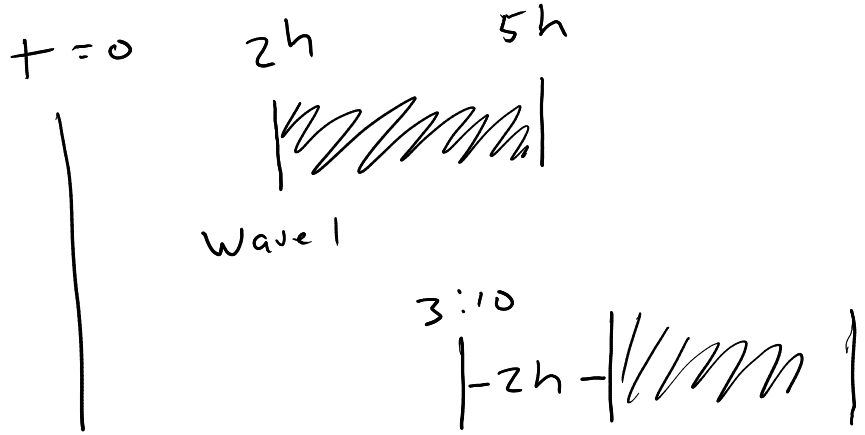
In each race, the fastest runner will take at least **2 hours**, and the slowest runner will finish in **5 hours or less**.

Multiple races can use the course at once, but everyone from one race must finish before racers from the next race can finish.

It takes **10 minutes to reset** the finish line after the last runner crosses from each race.

How long will it take for all five races to finish?

Besides making people run faster, **how can you speed it up**?



17:40 total

ES 4: Timing combinational logic

Steven Bell

19 September 2024

Tufts UNIVERSITY

Some observations from lab

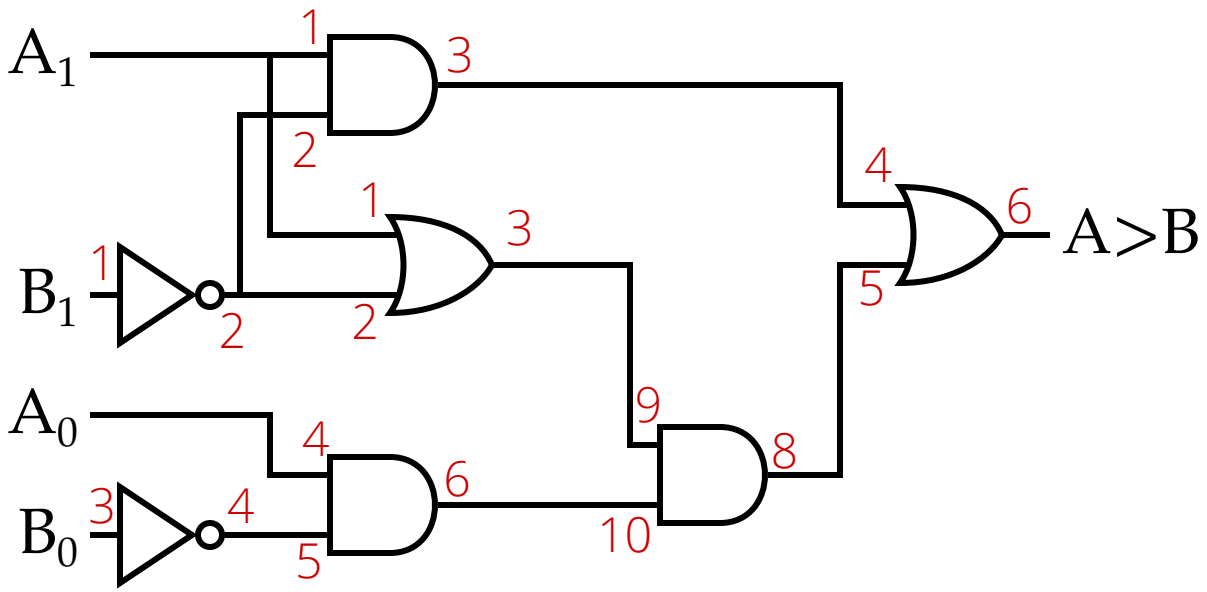
Many errors could be avoided

Slow and steady wins the race

Some observations from lab

Many errors could be avoided

Slow and steady wins the race



By the end of class today, you should be able to:

- Given a circuit and timing information about the gates, calculate the contamination delay and propagation delay
- Optimize a circuit for speed
- Explain what glitches are and why they occur

If electricity moves at the speed of light...

why are there delays at all?

and so timing depends on lots of things!

(excerpts from SN74LS04 datasheet)

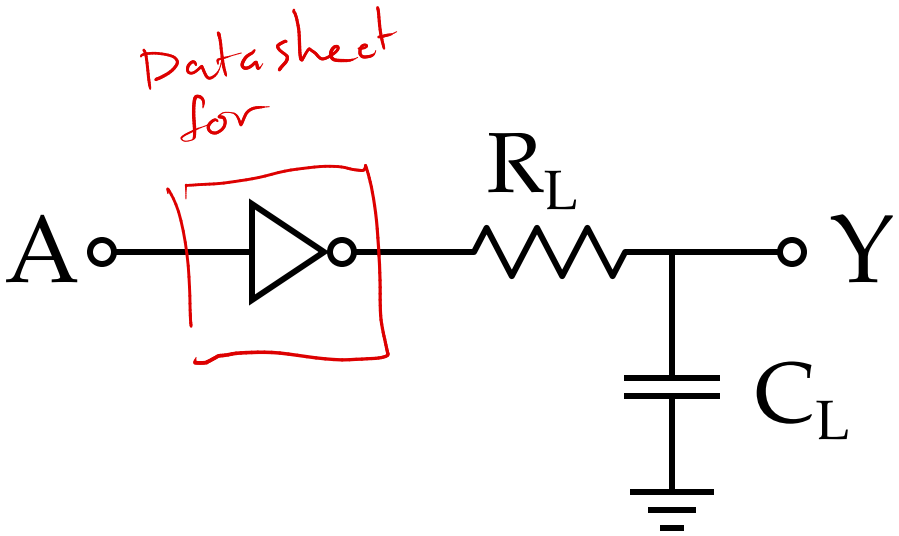
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5404 SN7404			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

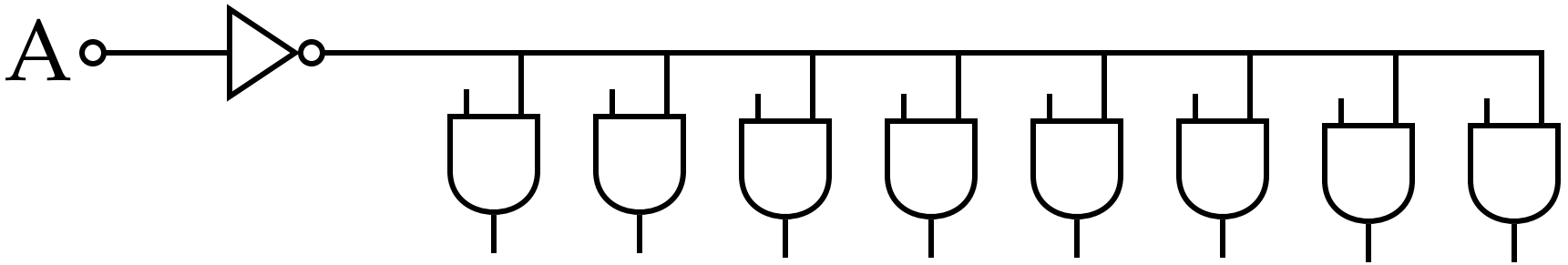
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S04 SN74S04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω, C_L = 15 pF		3	4.5	ns
t_{PHL}					3	5	
t_{PLH}	A	Y	R_L = 280 Ω, C_L = 50 pF		4.5		ns
t_{PHL}					5		

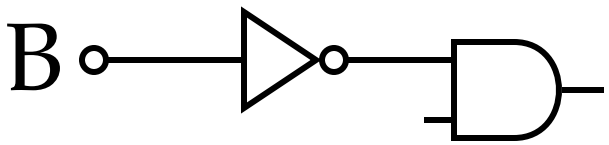
Test conditions??



Load (fanout) affects timing

Which inverter will switch faster?

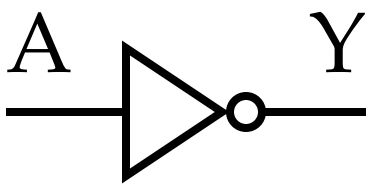


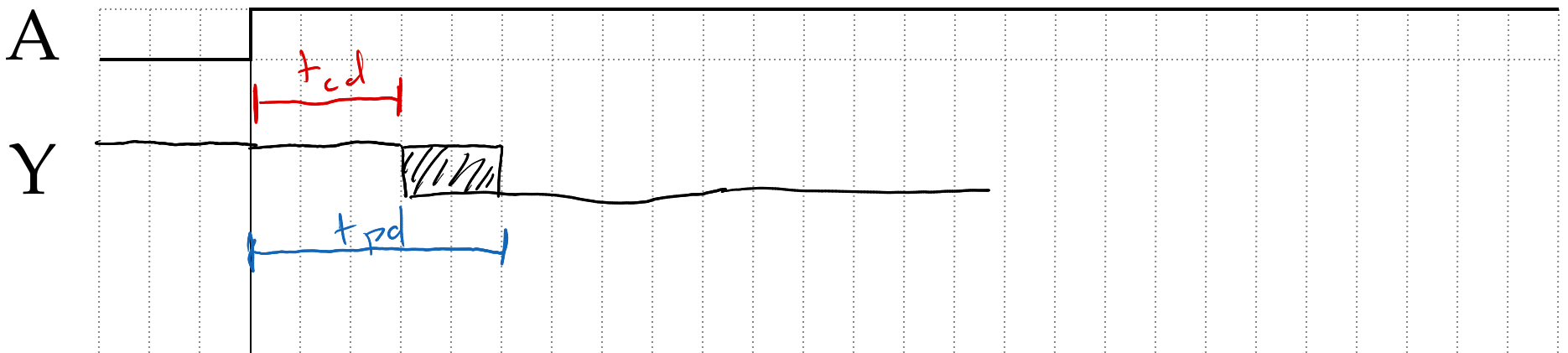


Timing

Contamination delay: the soonest that the output might change

Propagation delay: the maximum time for the output to settle

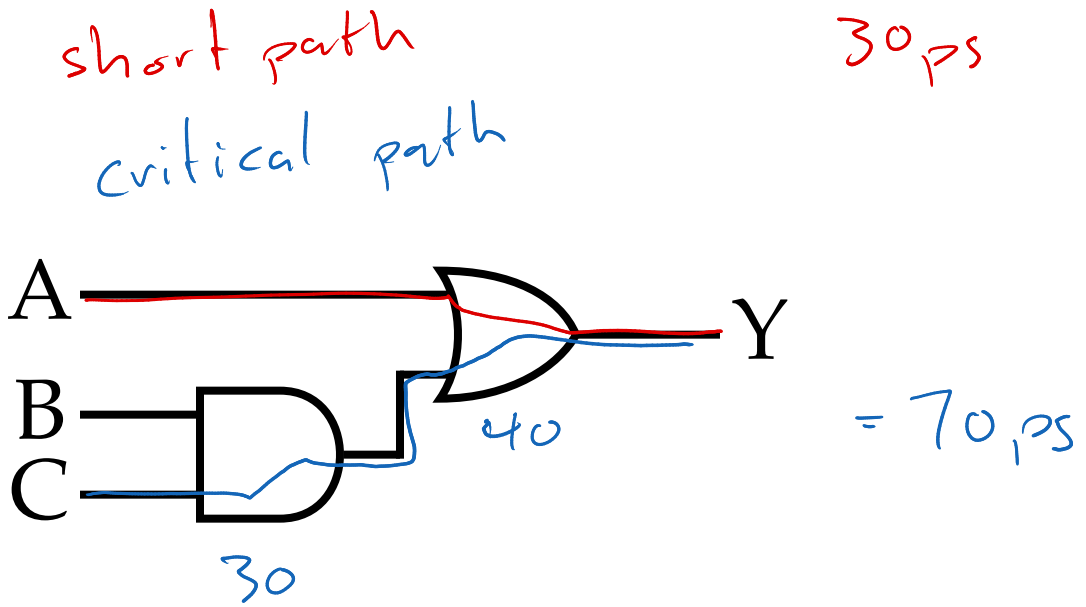




Timing practice

Find the contamination delay and propagation delay for this circuit

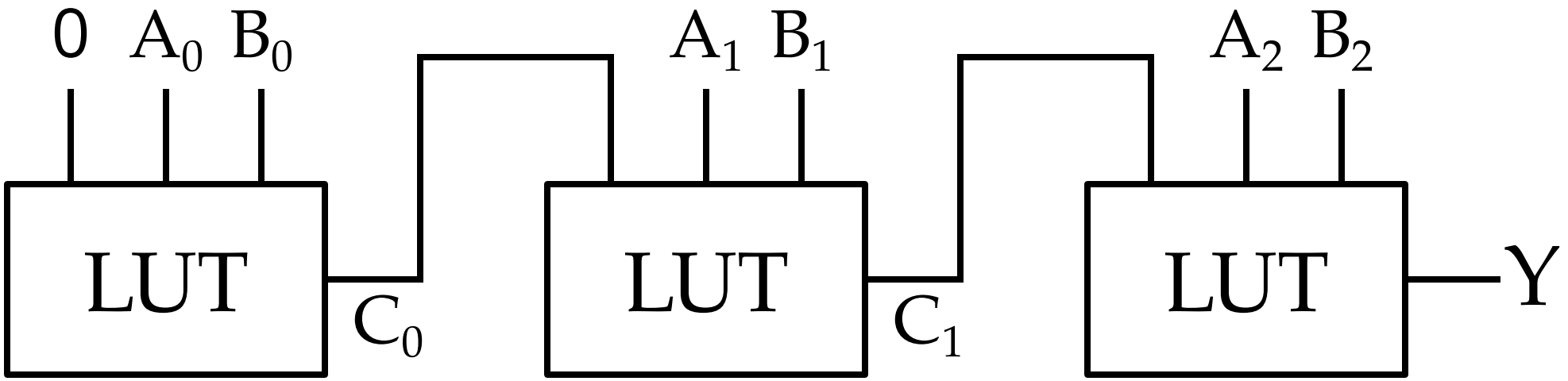
Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40



Timing practice

Find the worse-case propagation delay for this circuit

Assume the LUT has a delay of **10ns** from input (A/B) to output (C/Y)



30 ps total

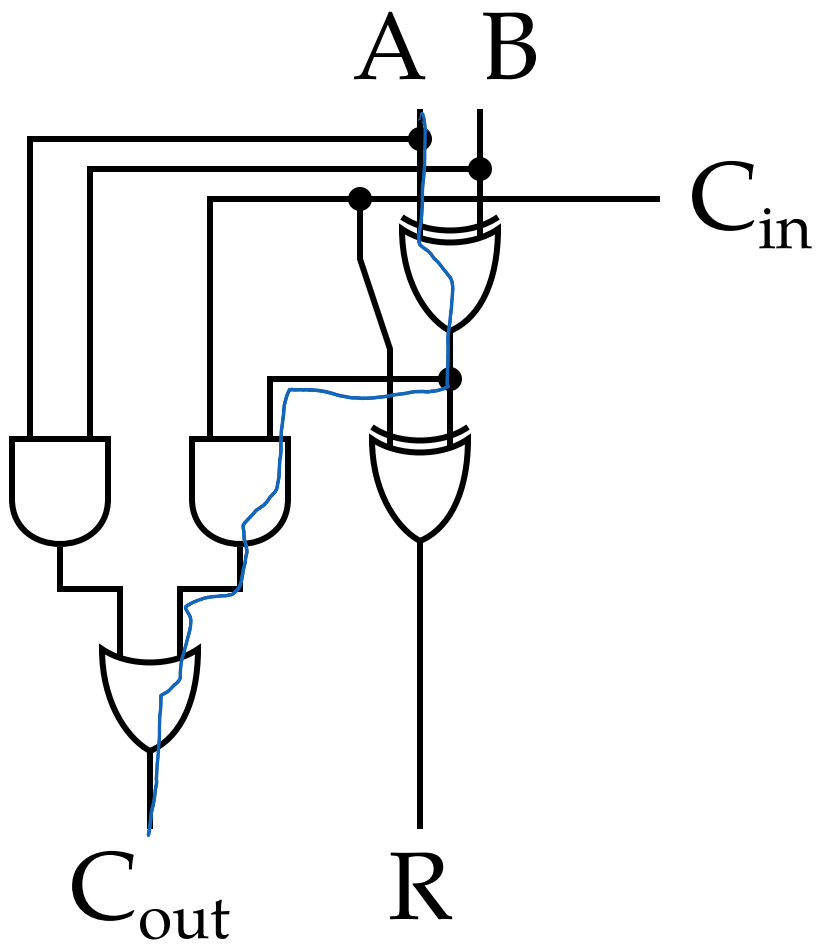
More practice!

Find the propagation delays for this circuit

R: 120 ps

Cout: 60 + 30 + 40 = 130 ps

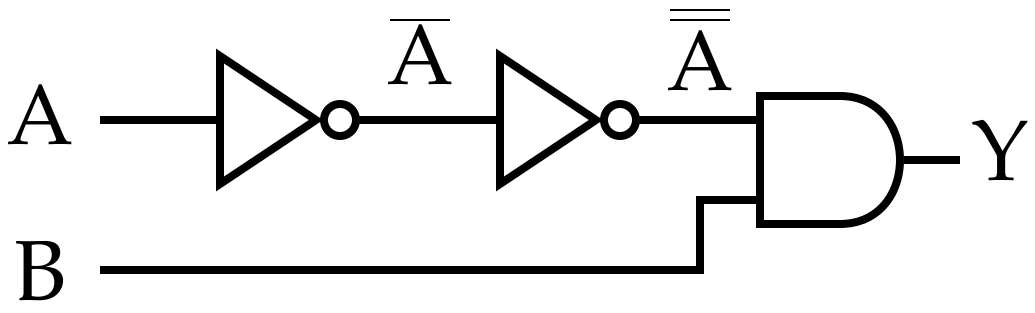
Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input NAND	20	15
3-input NAND	30	25
2-input NOR	30	25
3-input NOR	45	35
2-input AND	30	25
3-input AND	40	30
2-input OR	40	30
3-input OR	55	45
2-input XOR	60	40



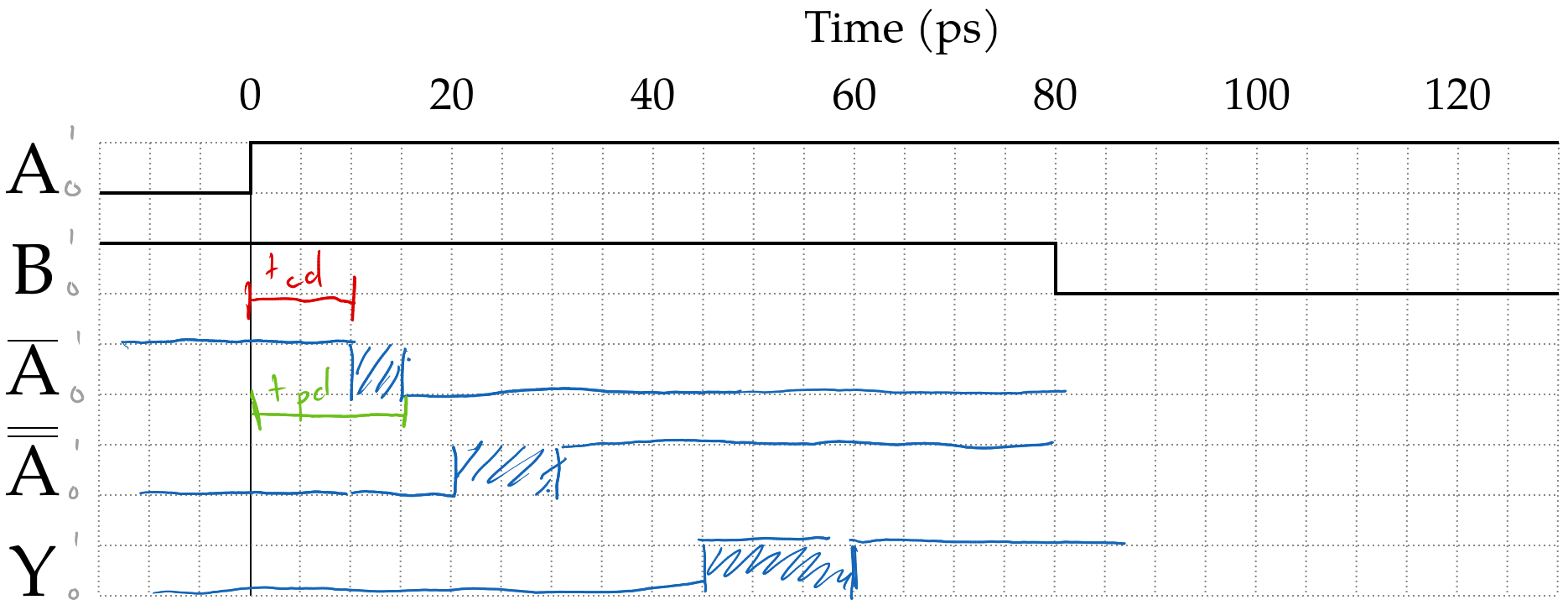
Who cares?

t_{cd} and t_{pd} combine to determine how fast the circuit can run.

Draw a timing diagram for these inputs:

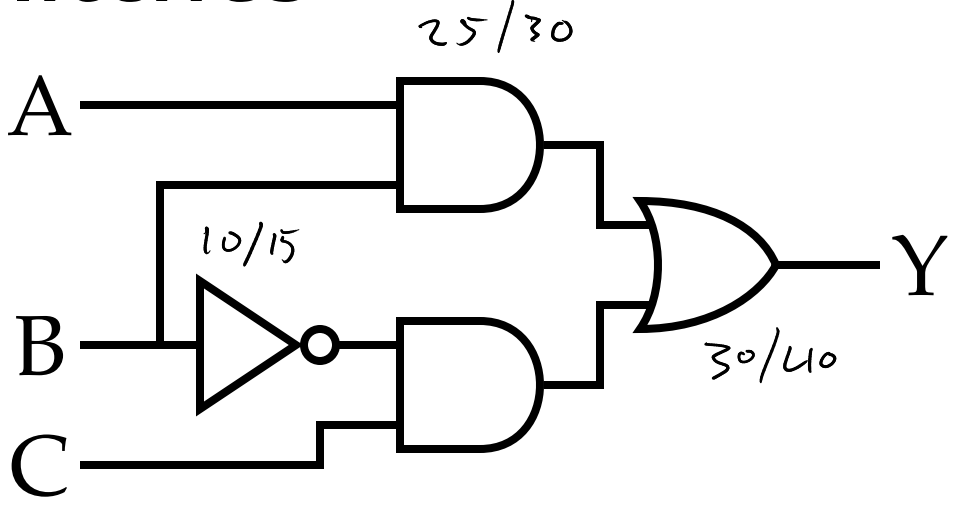


Gate	t_{pd} (ps)	t_{cd} (ps)
NOT	15	10
2-input AND	30	25

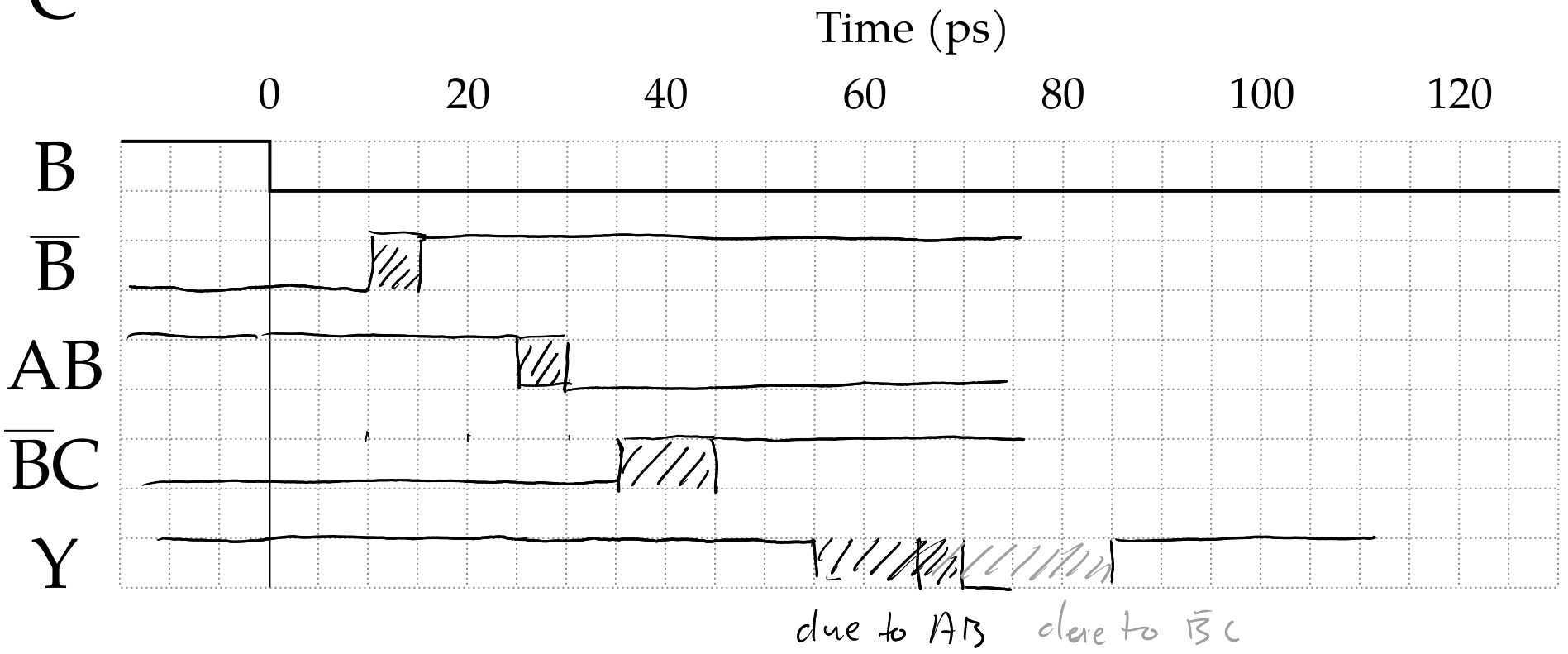


Glitches

(A and C are always high)



85 ps total




digital design
POWER TOOLS!

For next time

1. Read the book (4.1-4.2) and complete the reading check
2. Lab 3 prelabs due on Gradescope 24 hours in advance
3. Lab 2 reports due next week