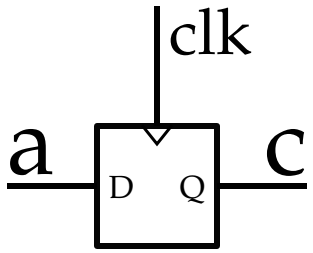
Warmup

Which circuit will be created by the VHDL below?

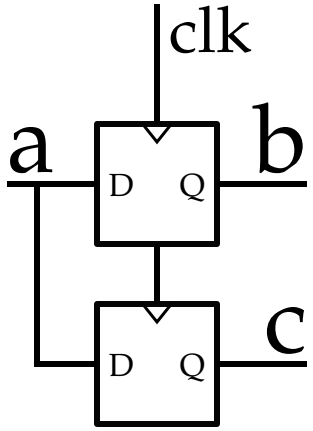
```
process (all) is
begin
   b <= a;
   c <= b;
end
```

(A)

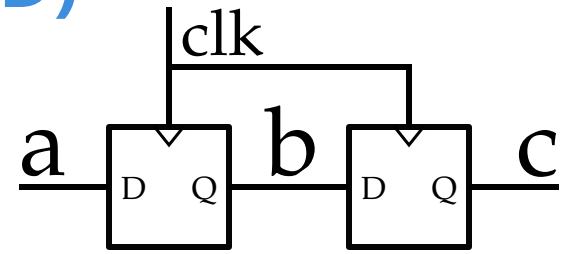


(B)

(C)



(D)



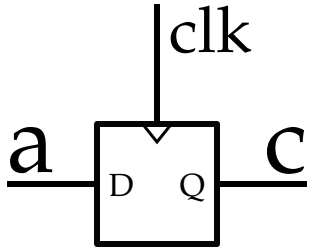
Respond at **pollev.com/stevenbell**

Warmup

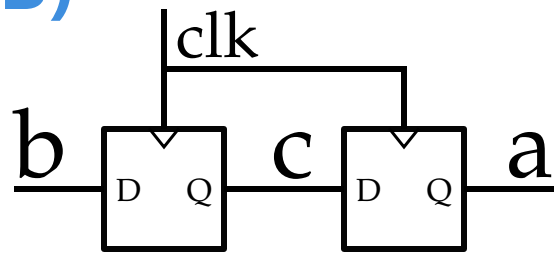
Which circuit will be created by the VHDL below?

```
process (clk) is
begin
  if rising_edge(clk) then
    c <= b;
    b <= a;
  end if;
end
```

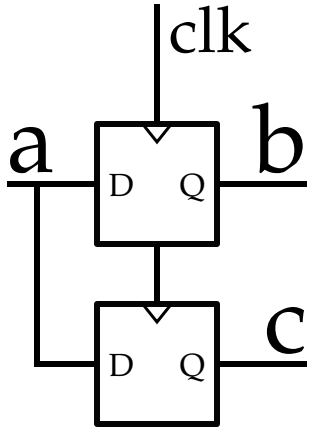
(A)



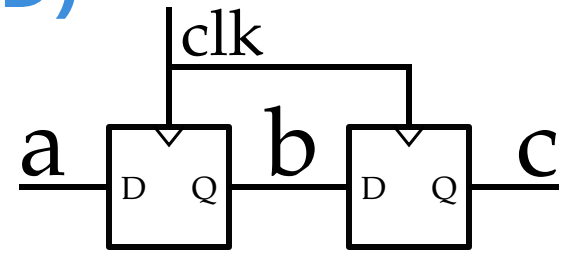
(B)



(C)



(D)



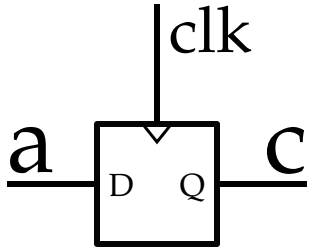
Respond at **pollev.com/stevenbell**

Warmup

Which circuit will be created by the VHDL below?

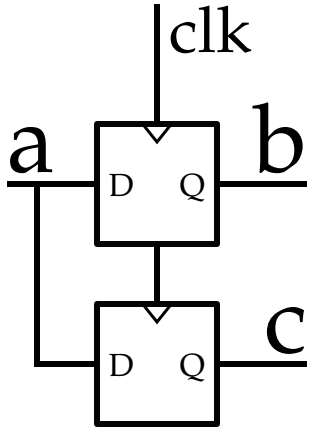
```
process (clk) is
begin
  if rising_edge(clk) then
    b <= a;
    c <= b;
  end if;
end
```

(A)

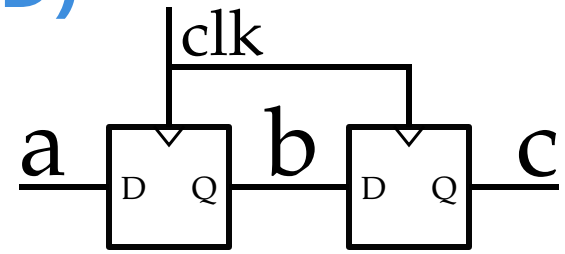


(B)

(C)



(D)



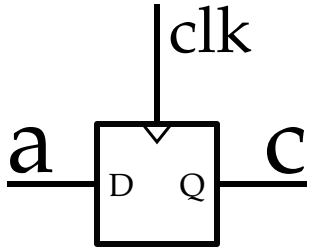
Respond at **pollev.com/stevenbell**

Warmup

Which circuit will be created by the VHDL below?

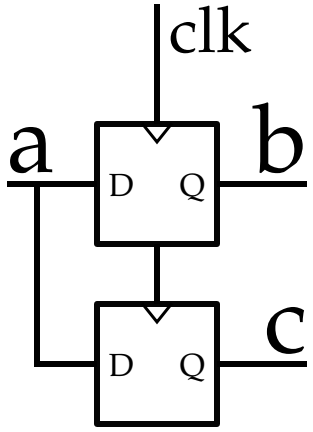
```
c <= b;
process (clk) is
begin
  if rising_edge(clk) then
    b <= a;
  end if;
end process;
```

(A)

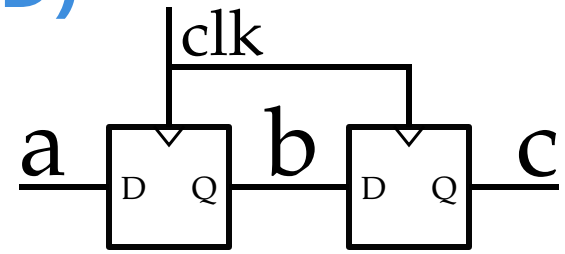


(B)

(C)



(D)



Respond at **pollev.com/stevenbell**

Port map

What is the purpose of the `port map` construct in VHDL?
Explain to your 4-week-younger self what `port map` does.

Respond at **pollev.com/stevenbell**

ES 4: State machines, part 2

Steven Bell

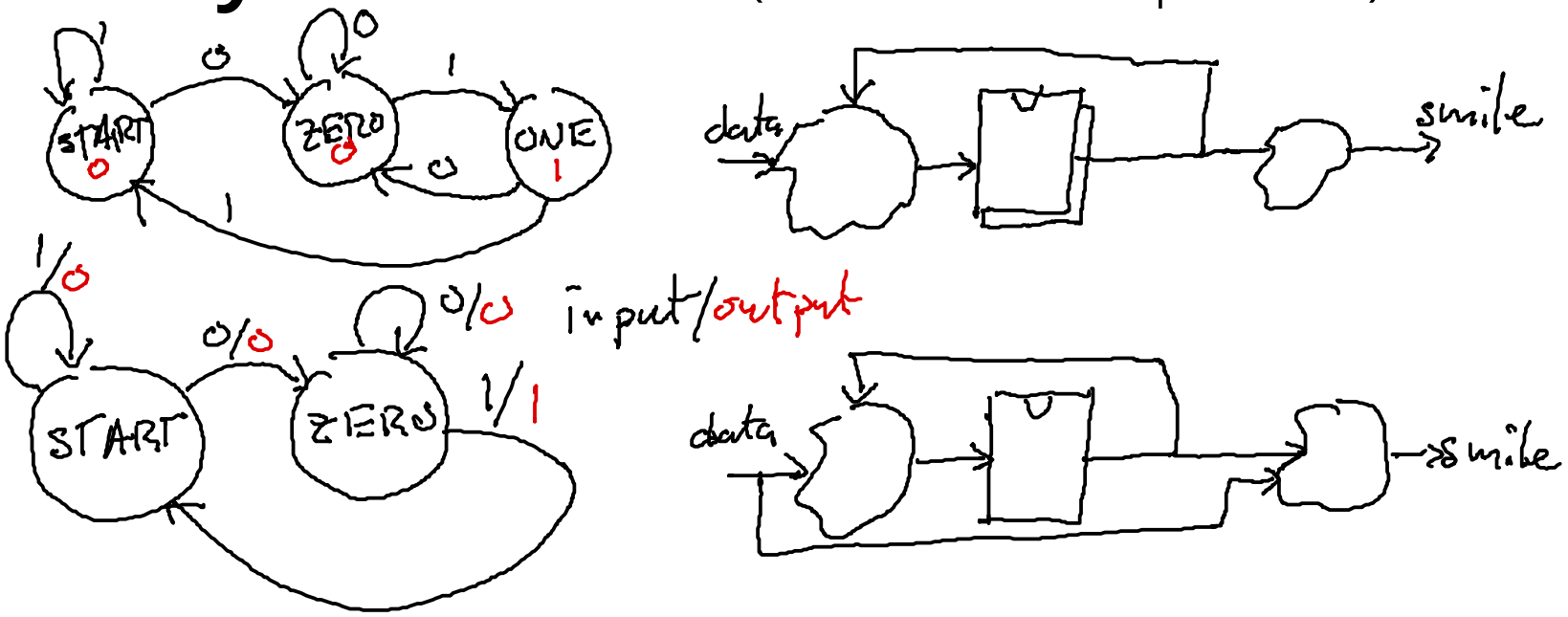
3 November 2021

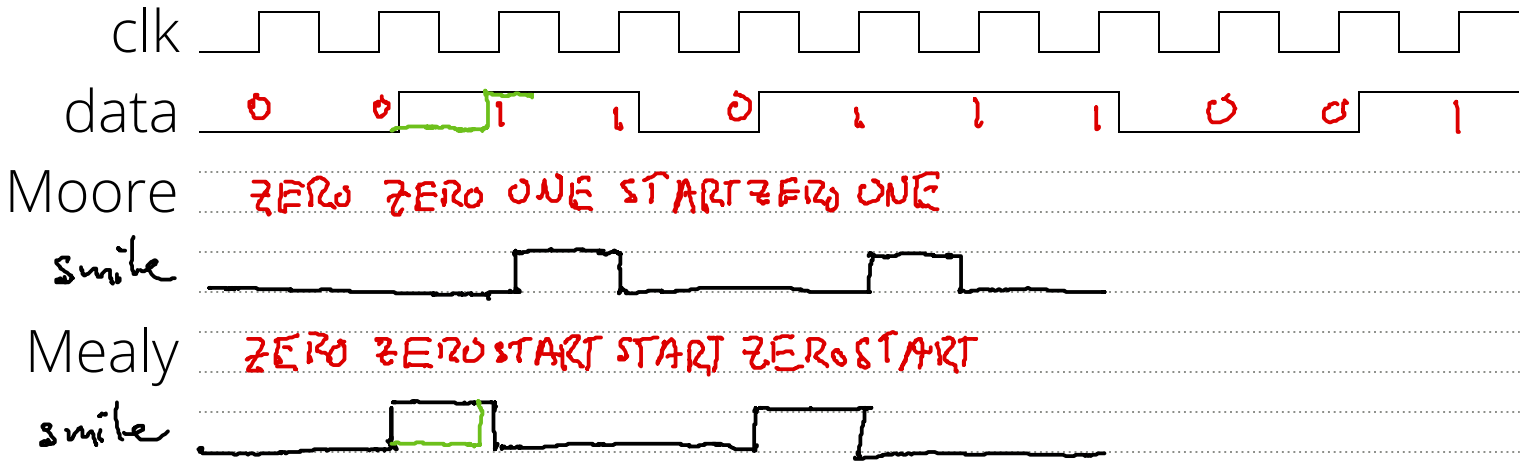
Tufts UNIVERSITY

Thanksgiving break

- Exam 2 will be on Nov 17 (Wednesday before break)
- You're invited to my house if you don't have plans

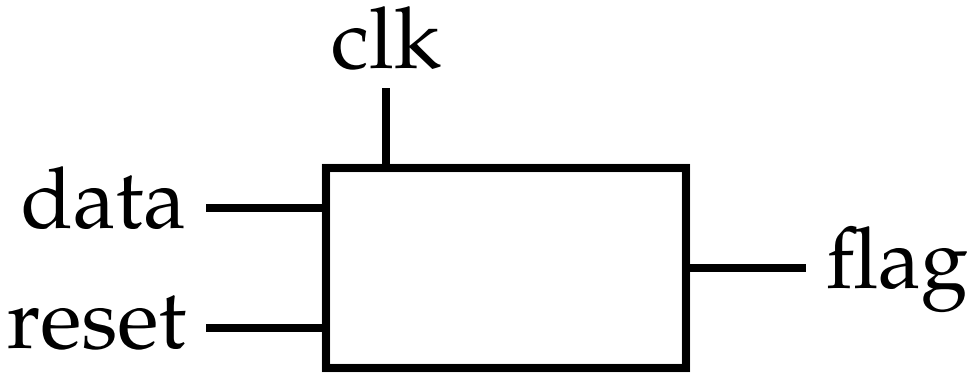
Mealy vs Moore (Harris example 3.7)





FSMs in VHDL

Design a circuit which sets a flag high when the "data" input has been high for 3 clock cycles. The flag should stay high until the reset signal is asserted (i.e., = 1)



FSM code: entity

FSM code: architecture

FSM code: state logic (inside architecture)

FSM code: output logic

Block diagrams

Which block diagram corresponds to the VHDL below?

```
entity blob is
  port (
    switch : in std_logic;
    count : out std_logic_vector(3 downto 0);
    valid : out std_logic
  );
end blob;
```

(A)

(B)

(C)

(D)

Respond at **pollev.com/stevenbell**