Warmup

Imagine we're playing a bizarre game called "musical cameras"

There are cameras around the room, which simultaneously take pictures every 5 seconds. You want to be in front of a new camera for every shot.

The autofocus for each camera takes 1 second. It takes you 0.5 seconds to hear the camera "click" and start moving.

You lose the game if any of your pictures come out blurry (because you arrived too late, or someone else moved too quickly and photobombed you).

How much time do you have to run between cameras?

ES 4: Sequential logic timing

Steven Bell

8 November 2021

Tufts UNIVERSITY

Simulating logic without VHDLweb

Questasim / Modelsim

- Available on Linux systems, via remote access, or lab VM
- Tutorial posted on course website

GHDL

- Download available for Windows/Mac/Linux
- Video tutorial posted on course website

Logistics

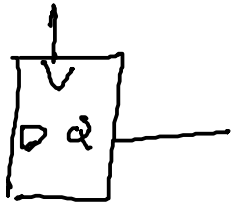
- Thursday lab sections meet on Tuesday (continue lab 6)
- Tuesday lab is "canceled", but Brandon will be there 4-6pm Tuesday
- Lab 7 will have multiple options, posted soon
- Late days and grades

By the end of class today, you should be able to

- Define **setup time** and **hold time**,
  and annotate them on a timing diagram
- Take a sequential circuit and a table of gate/FF delays, and **draw a timing diagram**.
- Calculate the **maximum frequency** a circuit can run at
- Calculate whether a circuit will have a **hold time violation**

Synchronizers and parallelism on Wednesday!

Terms



- **Clock-to-Q propagation delay** (t_{pcq})

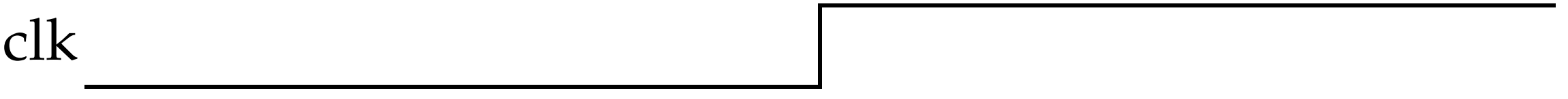
  Propagation delay from rising edge of clock to new value at Q

- **Setup time**

  Time before clock edge that FF needs to set up;
  input must be stable at least this much **before** clock edge.

- **Hold time**

  Time after clock edge that FF needs value to hold still;
  input must be stable at least this much **after** clock edge.

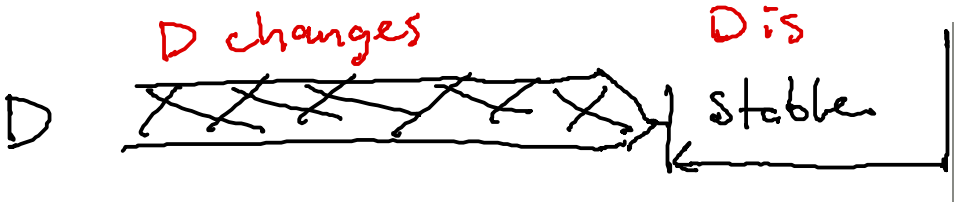


Clock-to-Q propagation delay (t_{pcq})

Propagation delay from rising edge of clock to new value at Q

Setup time

Input must be stable at least this much **before** clock edge.

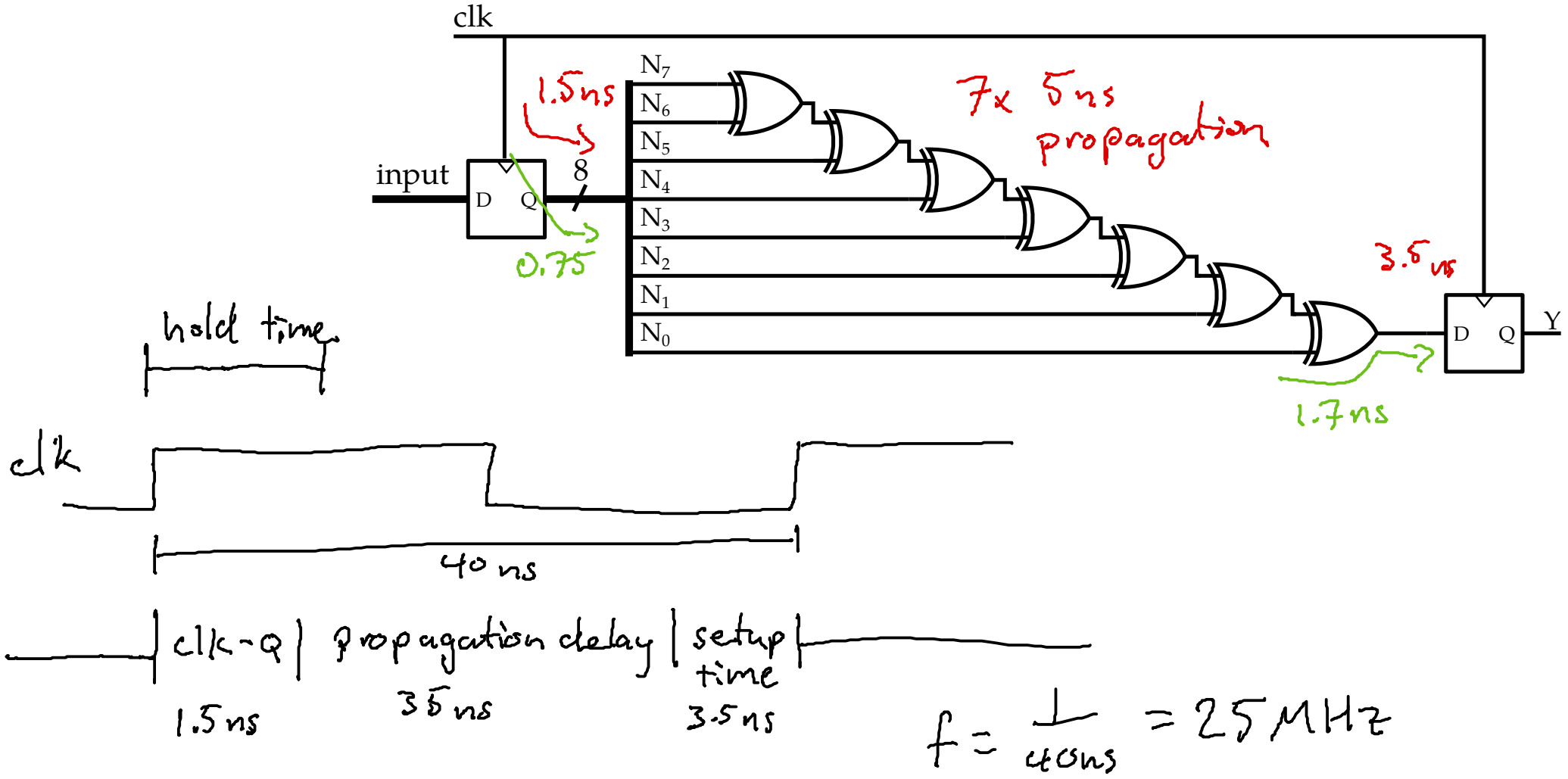


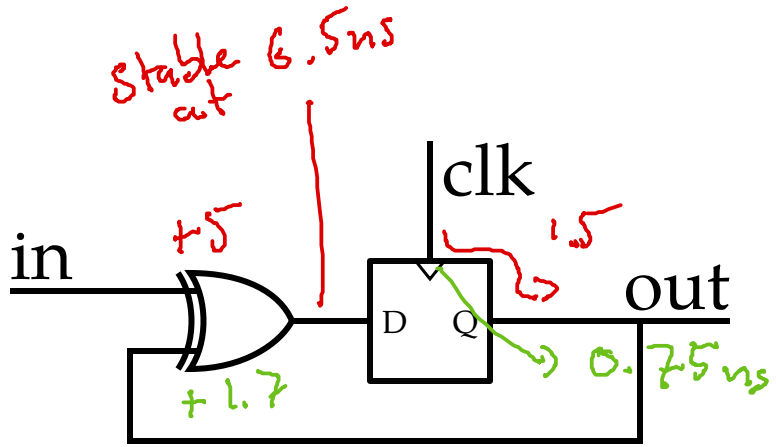
Hold time

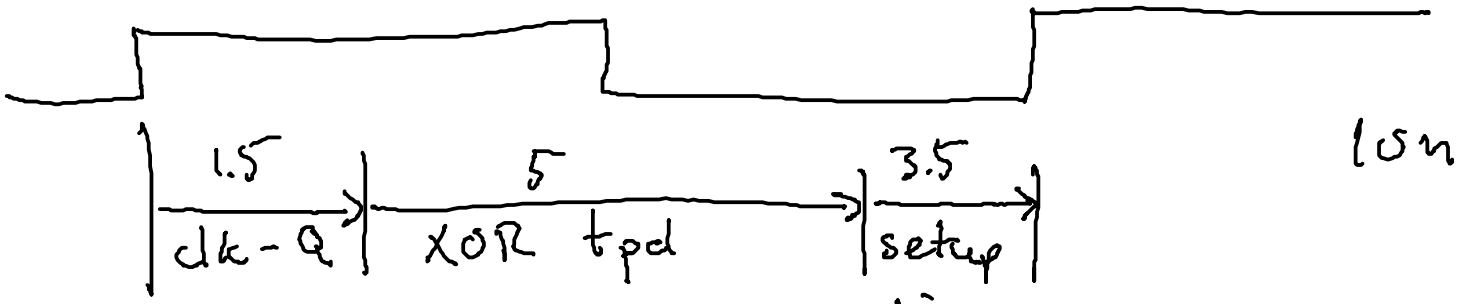
Input must be stable at least this much **after** clock edge.

How fast can this run?

(i.e., what is the maximum clock frequency before timing failure?)

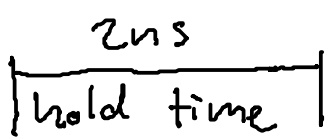



Stable 6.5ns
out
clk
in
+5
1.5
out
D
Q
0.75ns
+1.7



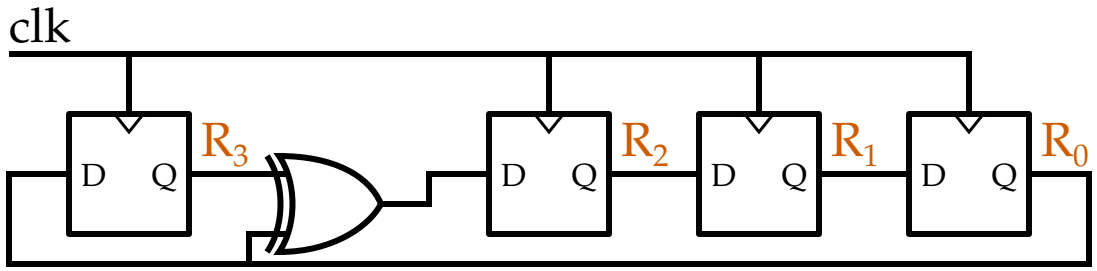
1.5
clk-Q
5
XOR tpd
3.5
setup
time

10ns = 100MHz


2ns
hold time


0.75
1.7ns

Can this run at 75 MHz?



Does this actually matter?

(Demonstration in Radiant)

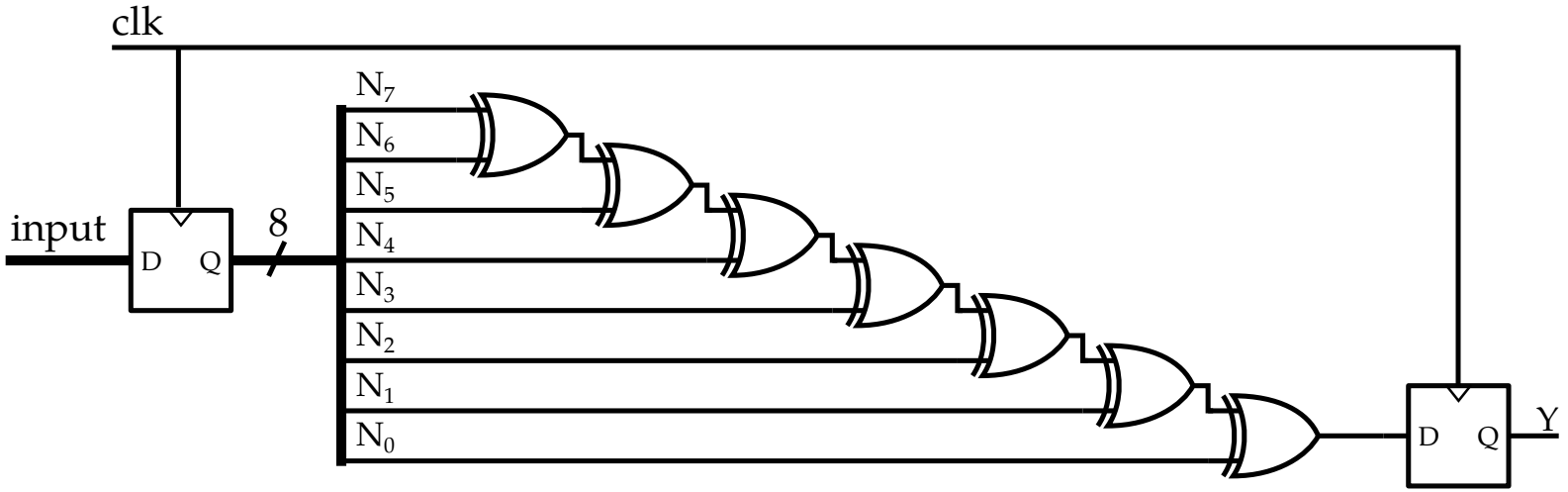
Those equations look pretty complicated; do we have to memorize them?

Those equations look pretty complicated;
do we have to memorize them?

Please don't.

You'll make your head hurt,
do poorly on the exam,
and forget all of it two months from now.

How do we speed this up?



For Wednesday

1. No reading! (We'll talk about 3.6 on Wednesday)

2. Go work on lab 6

3. Homework 6 will be posted eventually
   (and I'll give you appropriate time to complete it)