ES 4: Memory

Steven Bell

9 November 2023

Tufts UNIVERSITY

Logistics

- Exam 2 next Thursday
- Finish Lab 7 next week
- Look for an email from CATME for team assignment

Reading check questions

- I don't get bitlines and wordlines
- Why is RAM useful if it's volatile? (or, why pick RAM over ROM?)

By the end of class today, you should be able to

- Draw the general structure of a memory
- Describe the tradeoffs in memory between speed, storage, access, energy, and cost.
- Describe where register files, caches, DRAM, Flash, and spinning hard drives fit in the tradeoff space

Part 1: How is memory structured?

Part 1: How is memory structured?

Wordline activates a row (word) of the memory for reading/writing

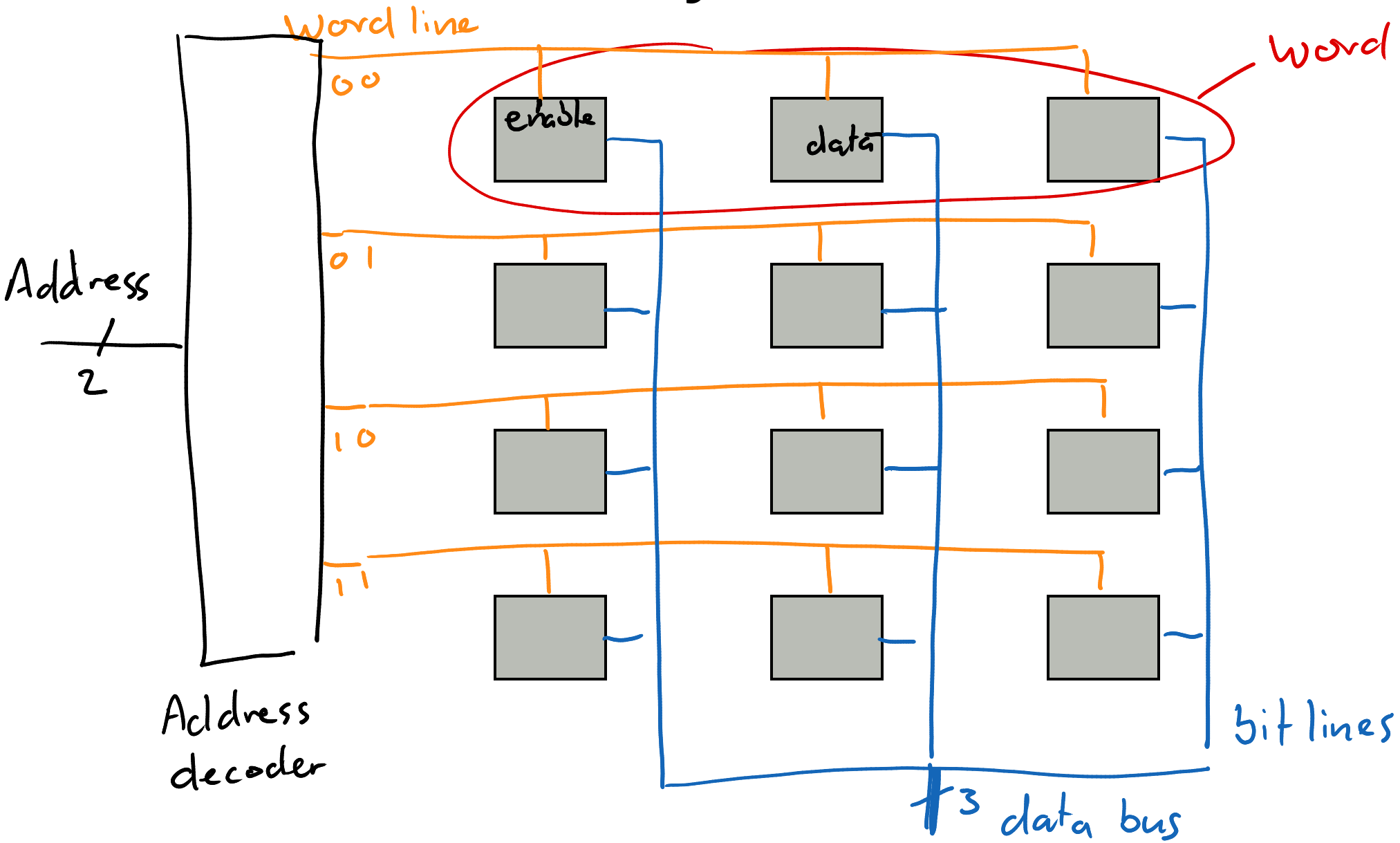
Bitline connects to a column, and reads/writes an individual bit

Address specifies which word of memory to operate on

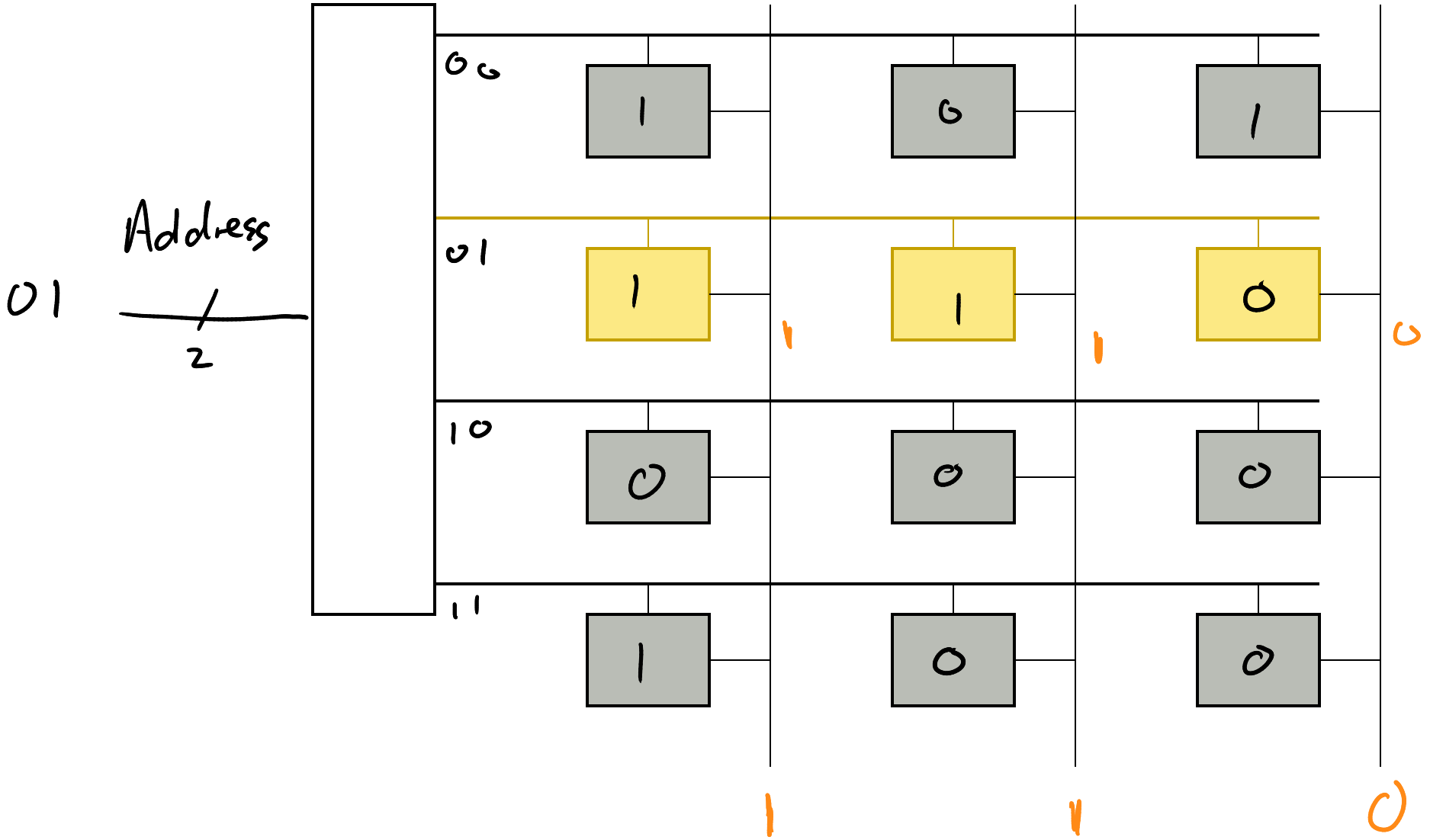
Decoder takes the address (as a binary number) and turns on the corresponding wordline

Data bus aggregates the bitlines to carry the complete word

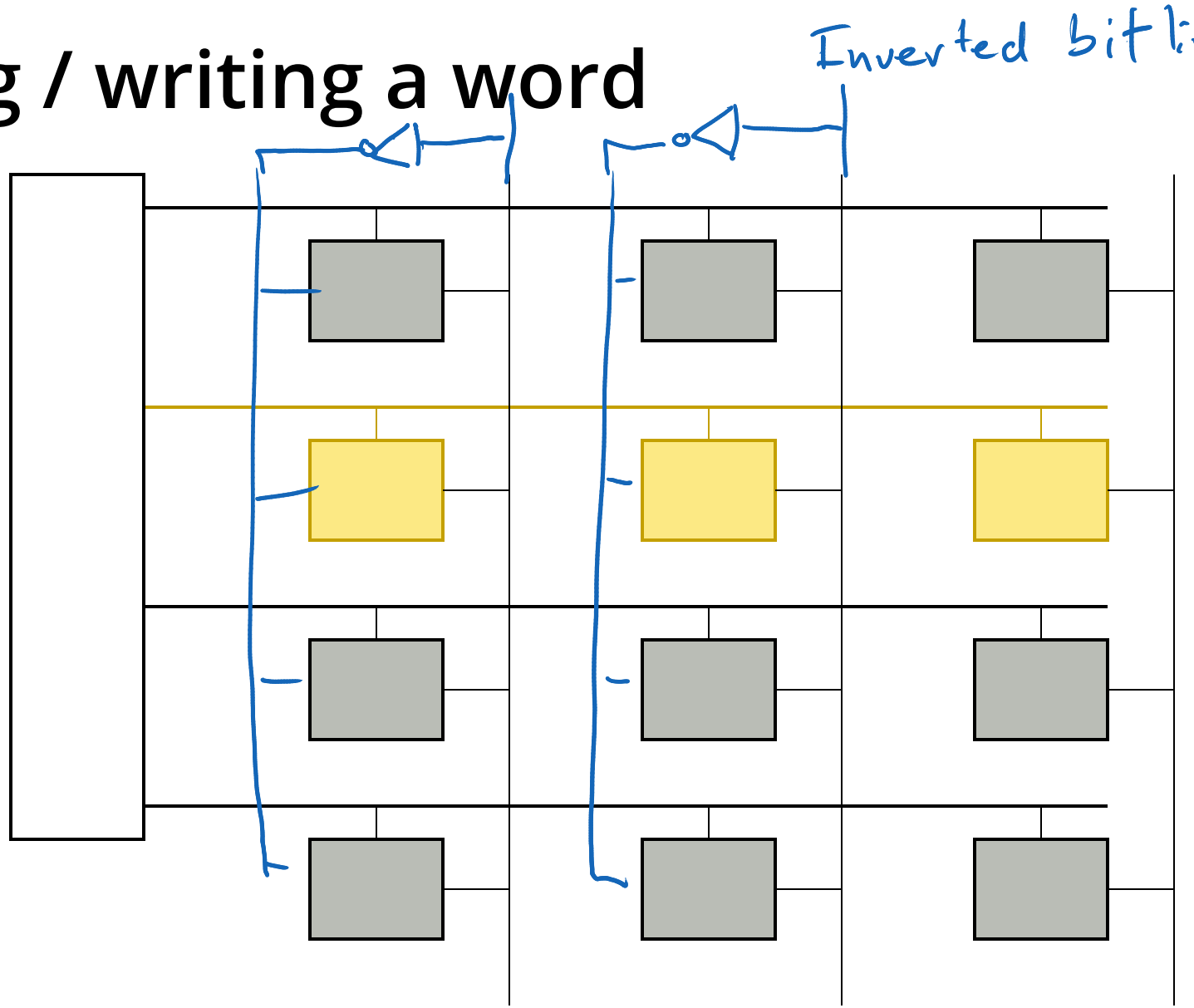
Part 1: How is memory structured?



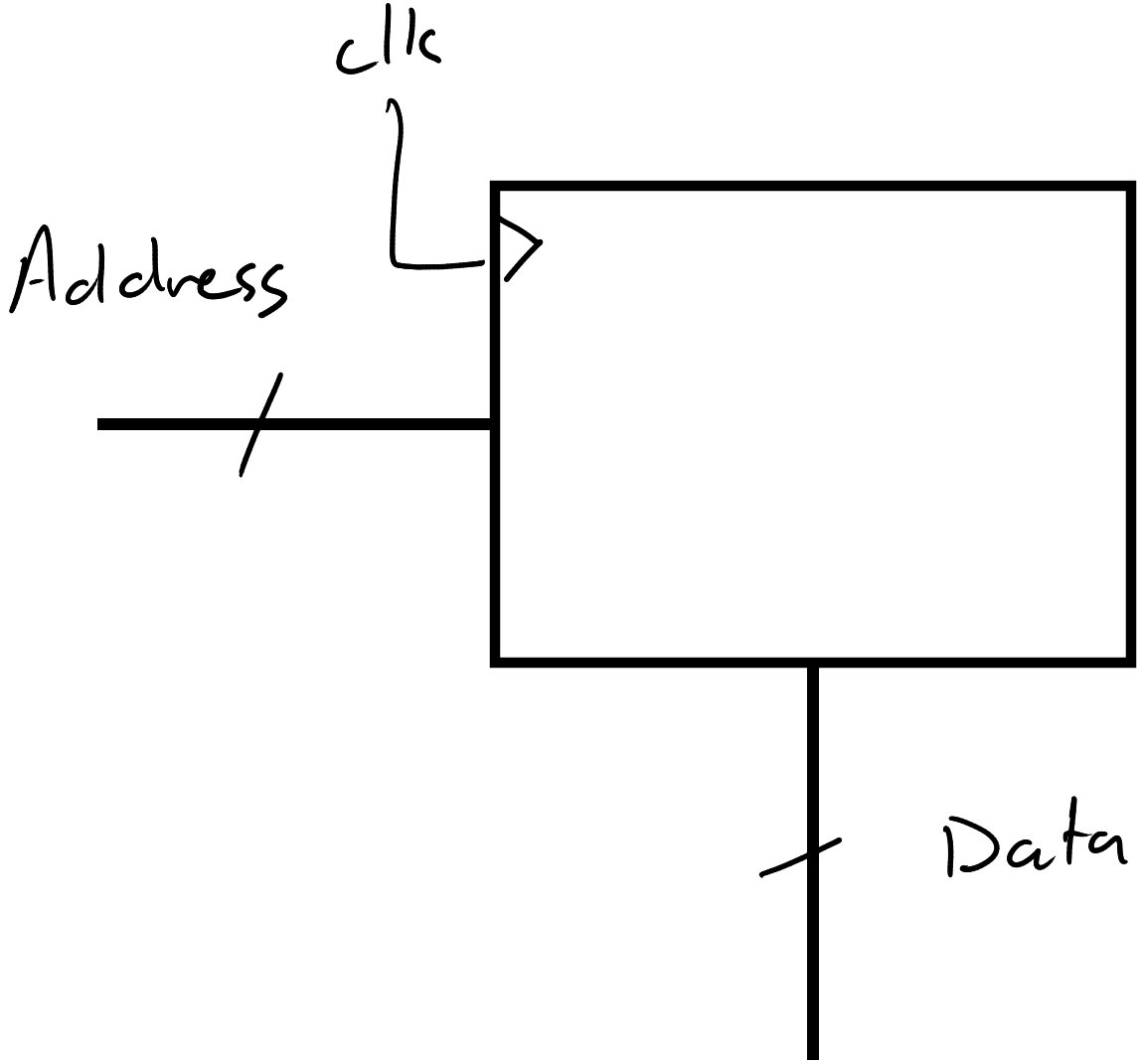
Reading / writing a word



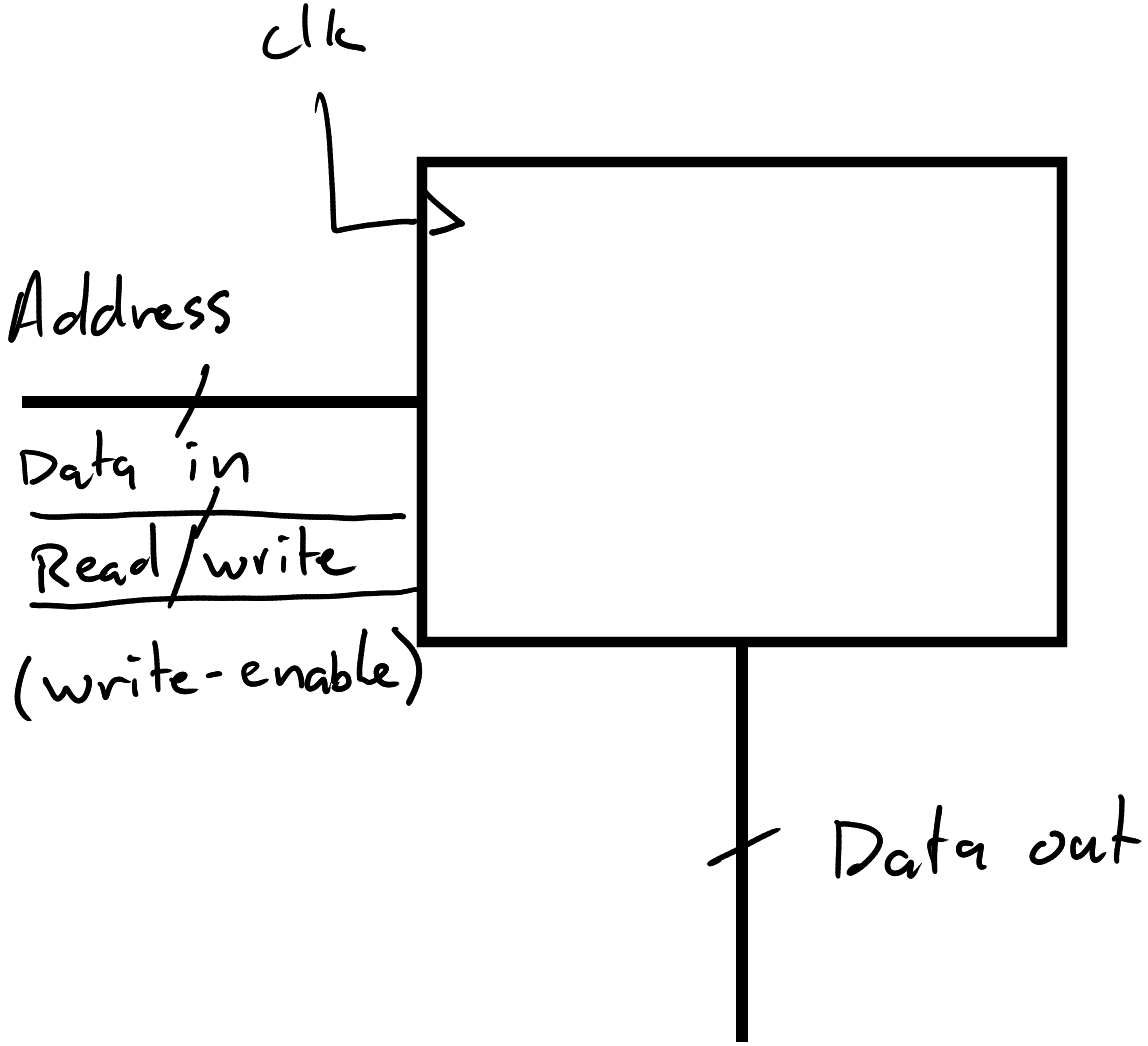
Reading / writing a word



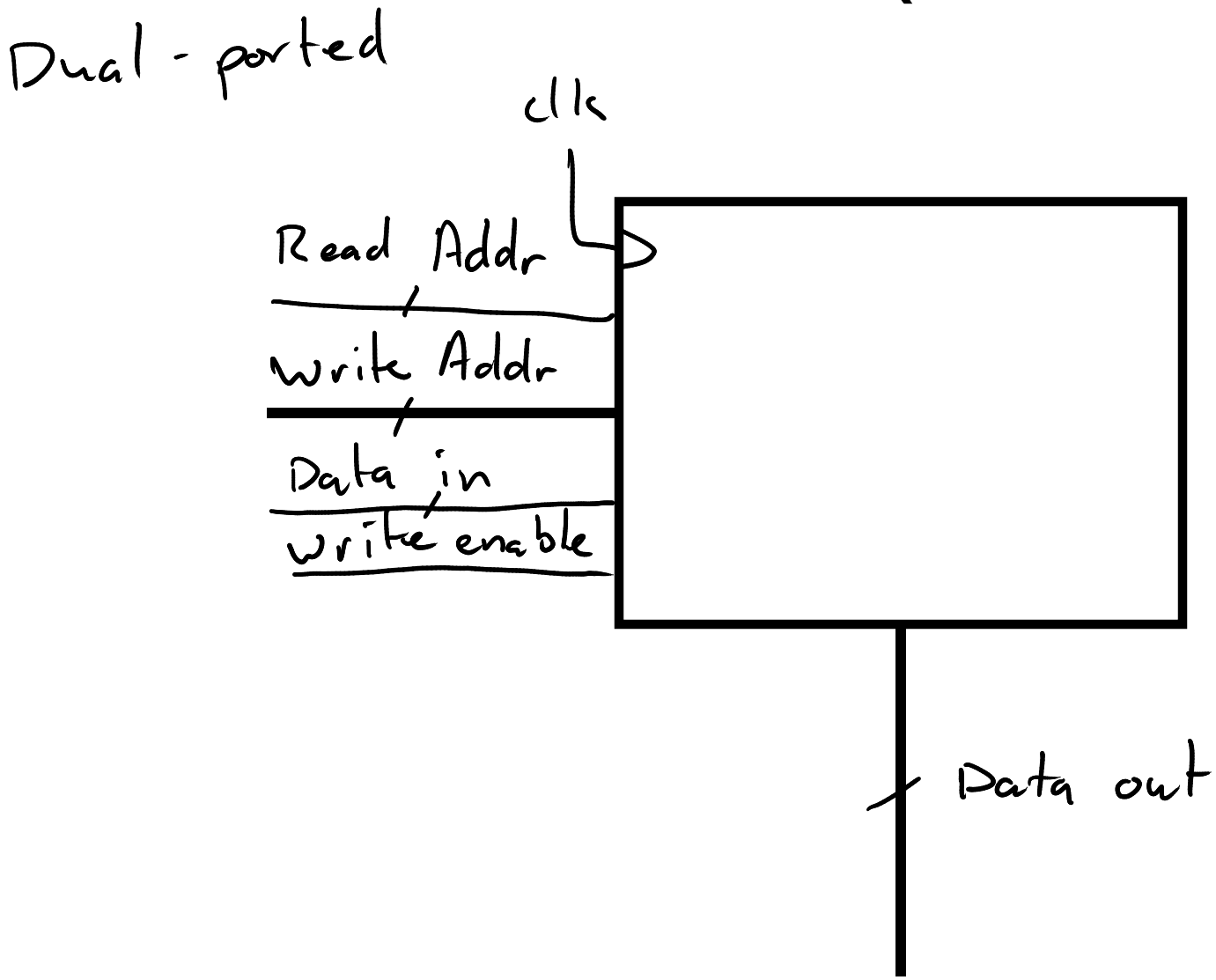
An abstracted view of (read-only) memory



An abstracted view of (read-write) memory



An abstracted view of (read-write) memory



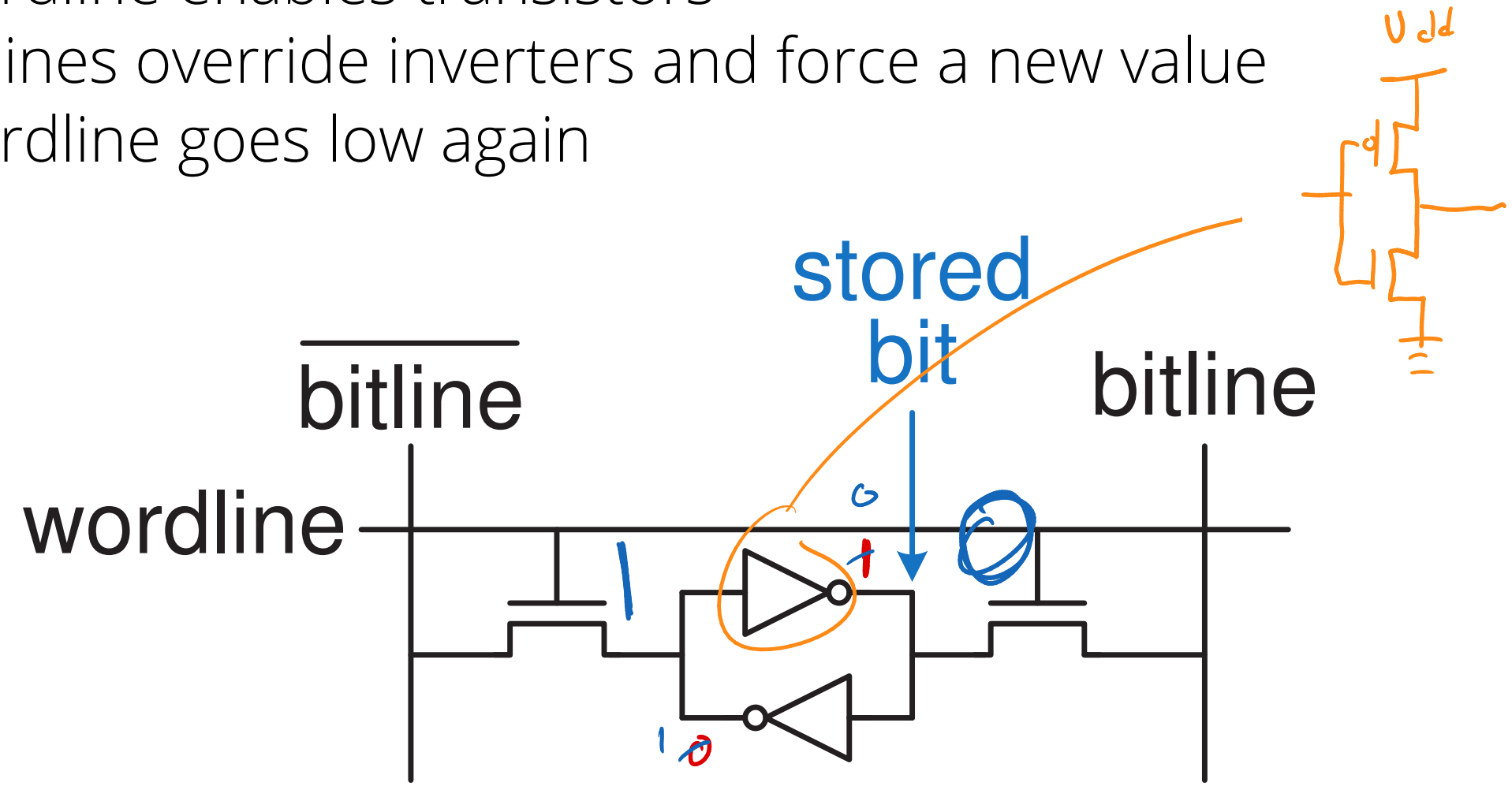
Part 2: Inside SRAM and DRAM

SRAM is "**static** random-access-memory"

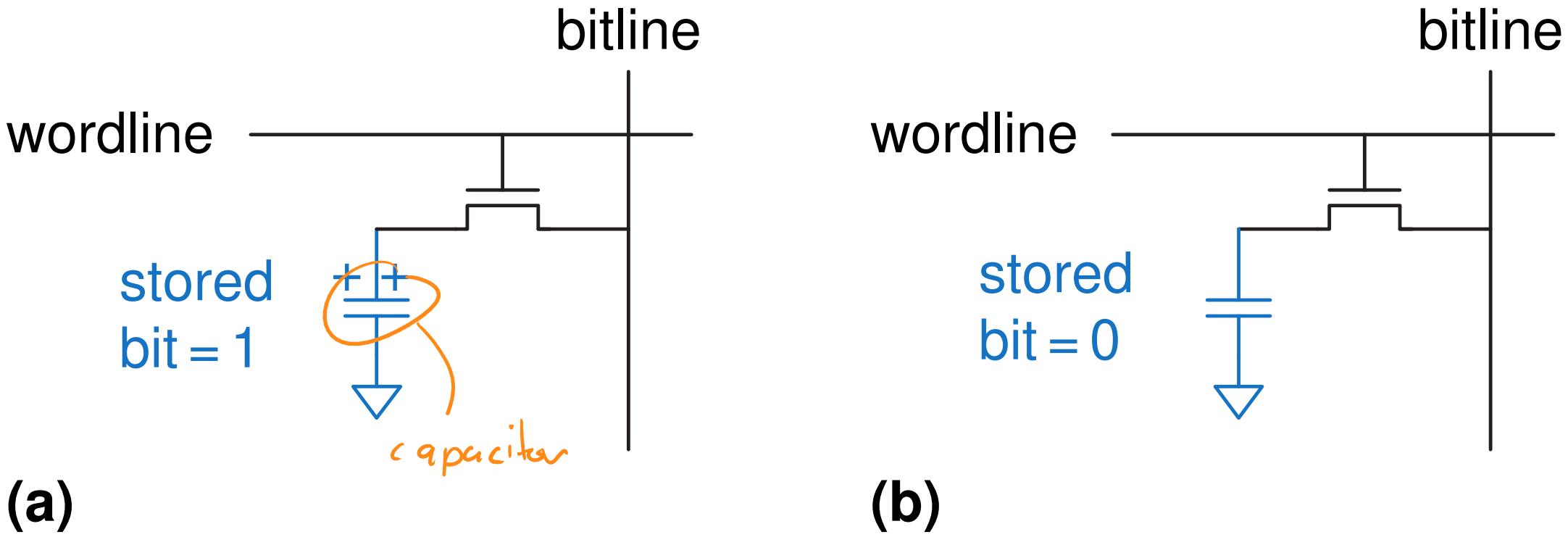
DRAM is "**dynamic** random-access-memory"

Inside SRAM

1) wordline enables transistors
2) bitlines override inverters and force a new value
3) wordline goes low again

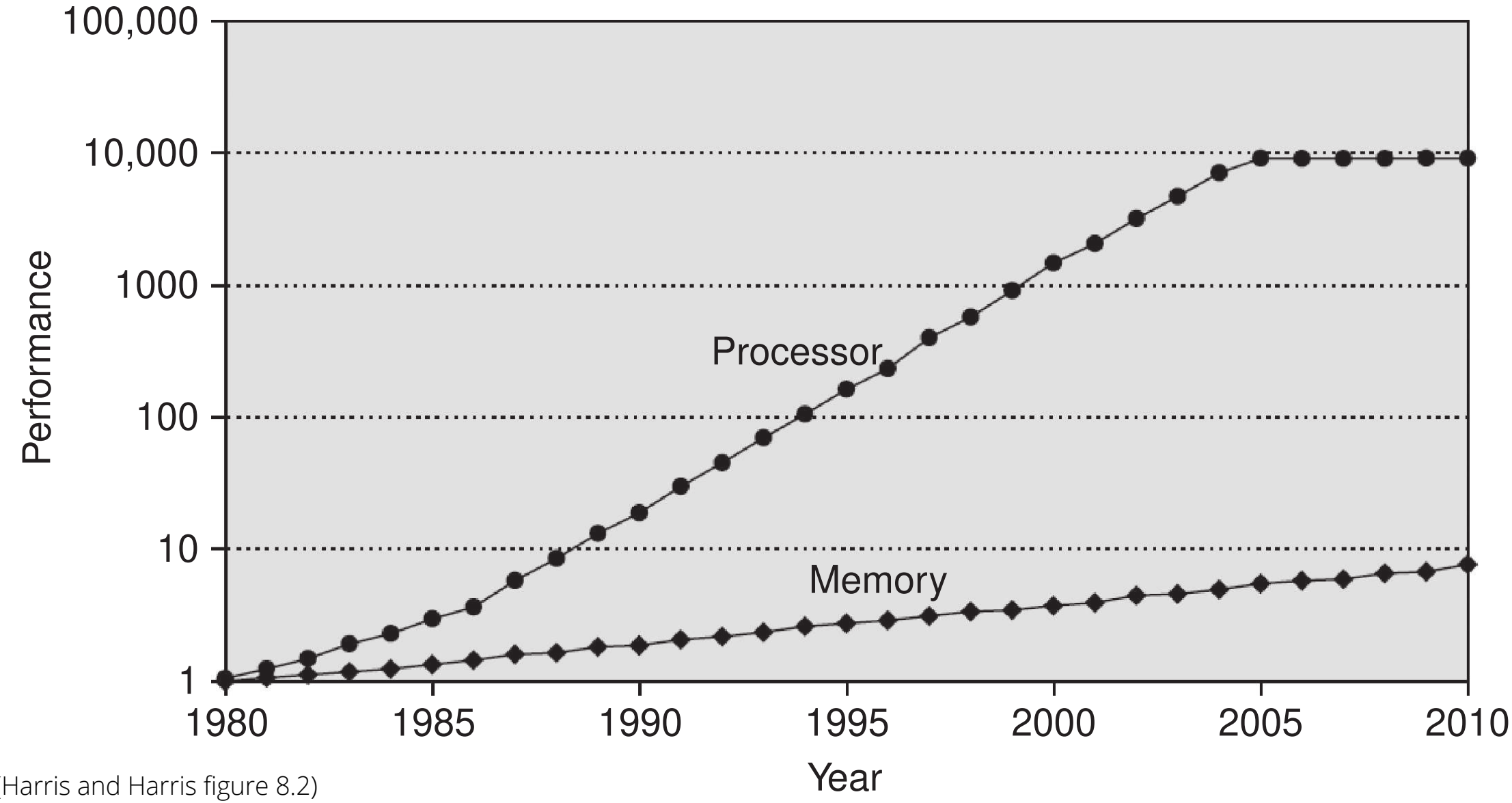


Inside DRAM


bitline
wordline
stored
bit = 1
capacitor
(a)
bitline
wordline
stored
bit = 0
(b)

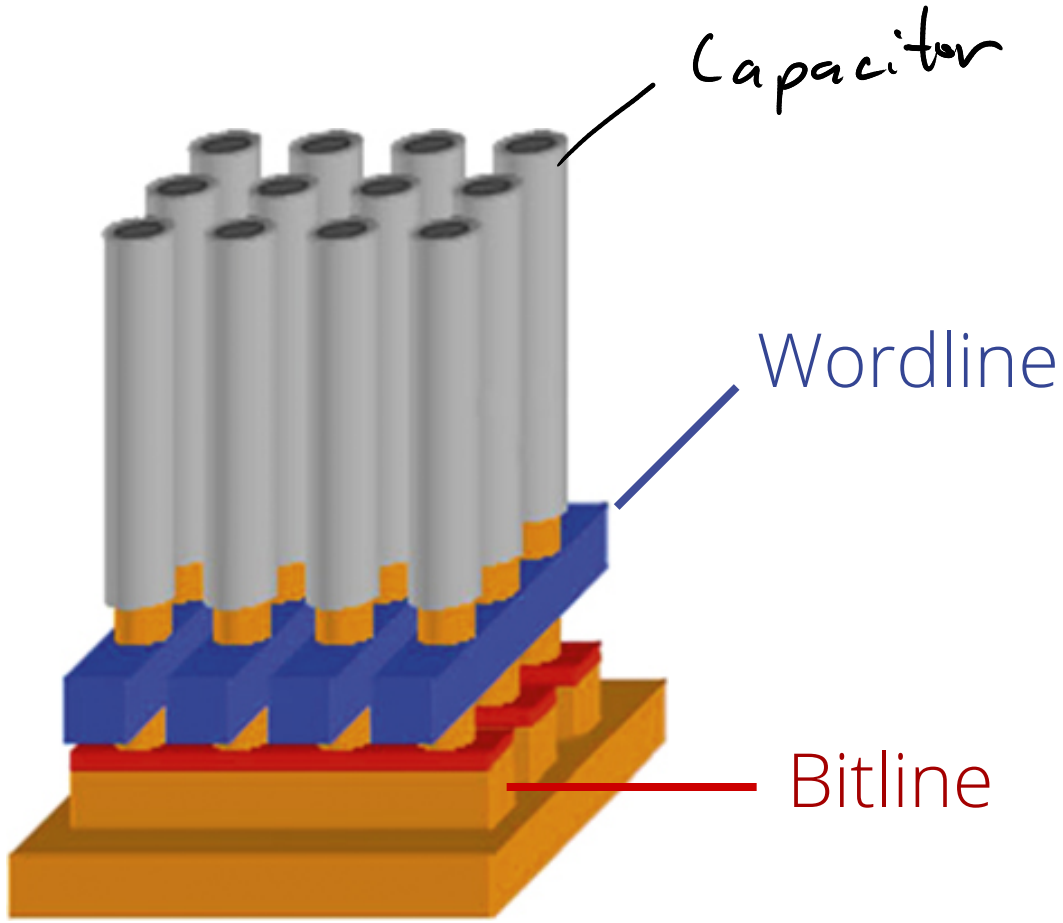
Part 3: Why do we need different kinds of memory?

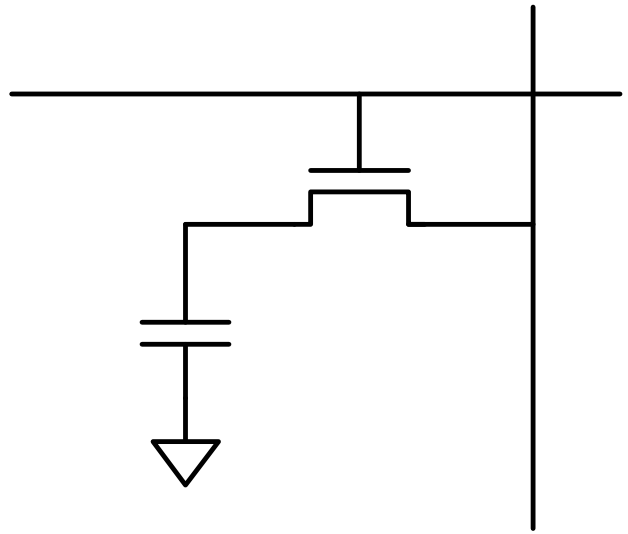
Memory (DRAM) vs CPU speeds



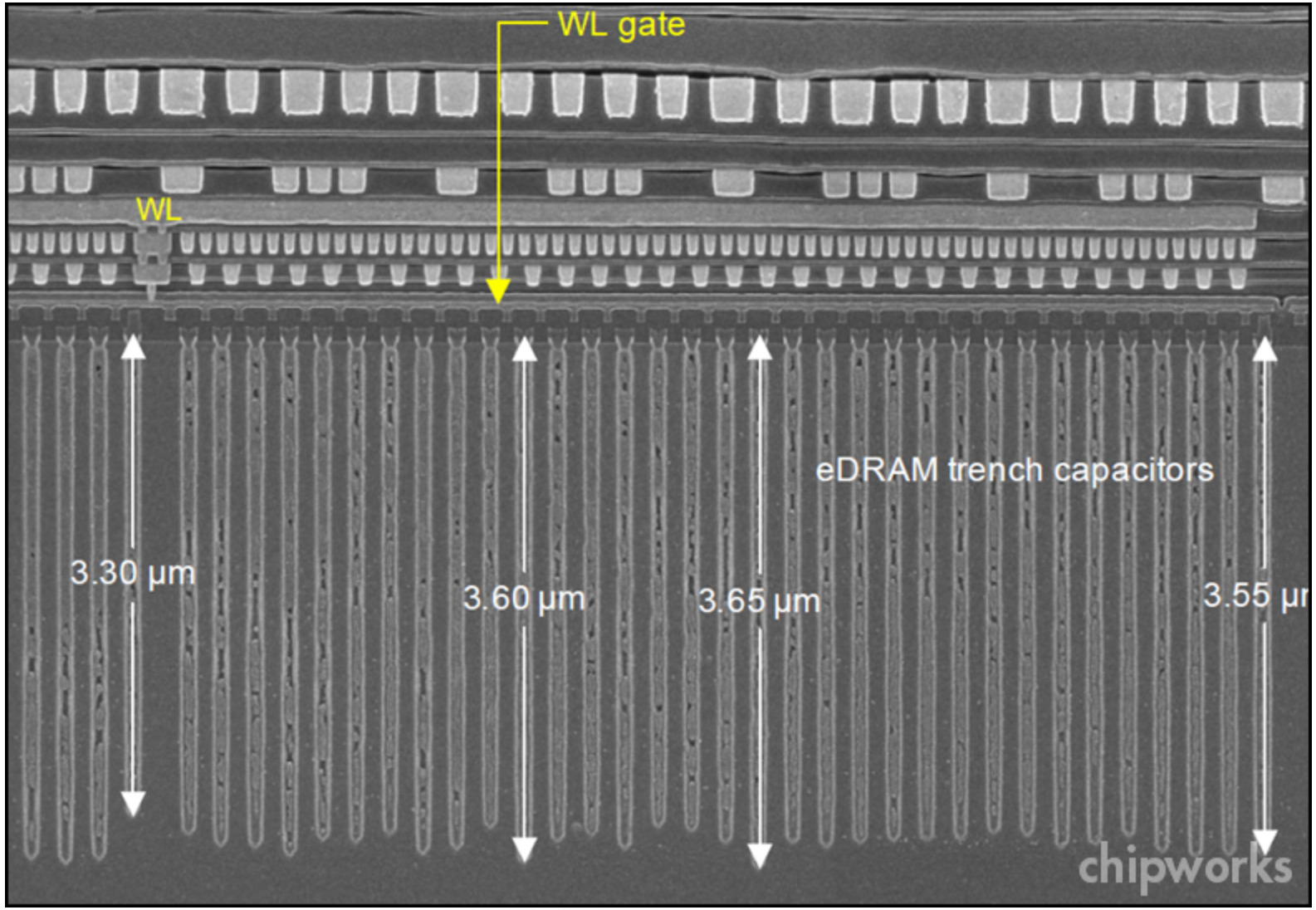
(Harris and Harris figure 8.2)

DRAM cell





DRAM cross section



(image from chipworks http://chipworksrealchips.blogspot.com/2014/02/intels-e-dram-shows-up-in-wild.html)

Comparing memory technologies

	SRAM			"solid state"	
	Register file	Cache	DRAM	Flash	Spinning disk
Cost/bit	$$$	$$$	$$	$	$
Speed	1 cycle	several cycles	hundreds of cycles	slow-ish	slow >10ms
Non-volatile	✗	✗	✗	✓	✓
Typical size	tens of registers ~2 kbit	few MB	tens GB	100+ GB	few TB

Tape drives?!

Memory in the FPGA

Just like a flip-flop: describe the behavior you want, and Radiant will "infer" the RAM/ROM for you.

For next time

1. Continue with lab 6

2. Look for CATME survey