ES 4: Memory

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Tufts UNIVERSITY

Logistics

- Exam 2 on Wednesday
- Lab 7 this week
- Ethics assignment due next Monday (work together!)
- Final project teams assigned on Wednesday

  Teams of 4 should email me by Wednesday if you want to work together, with a 1 paragraph proposal of what you want to do.

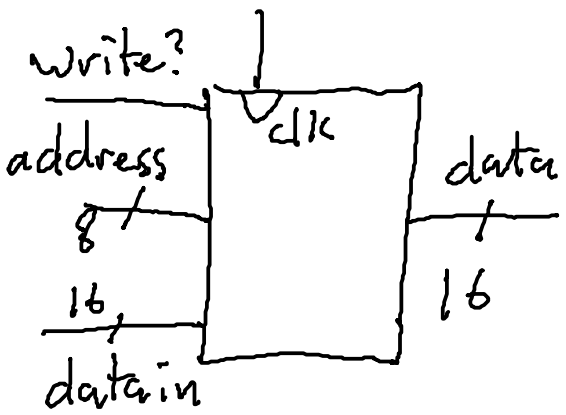
Reading check questions

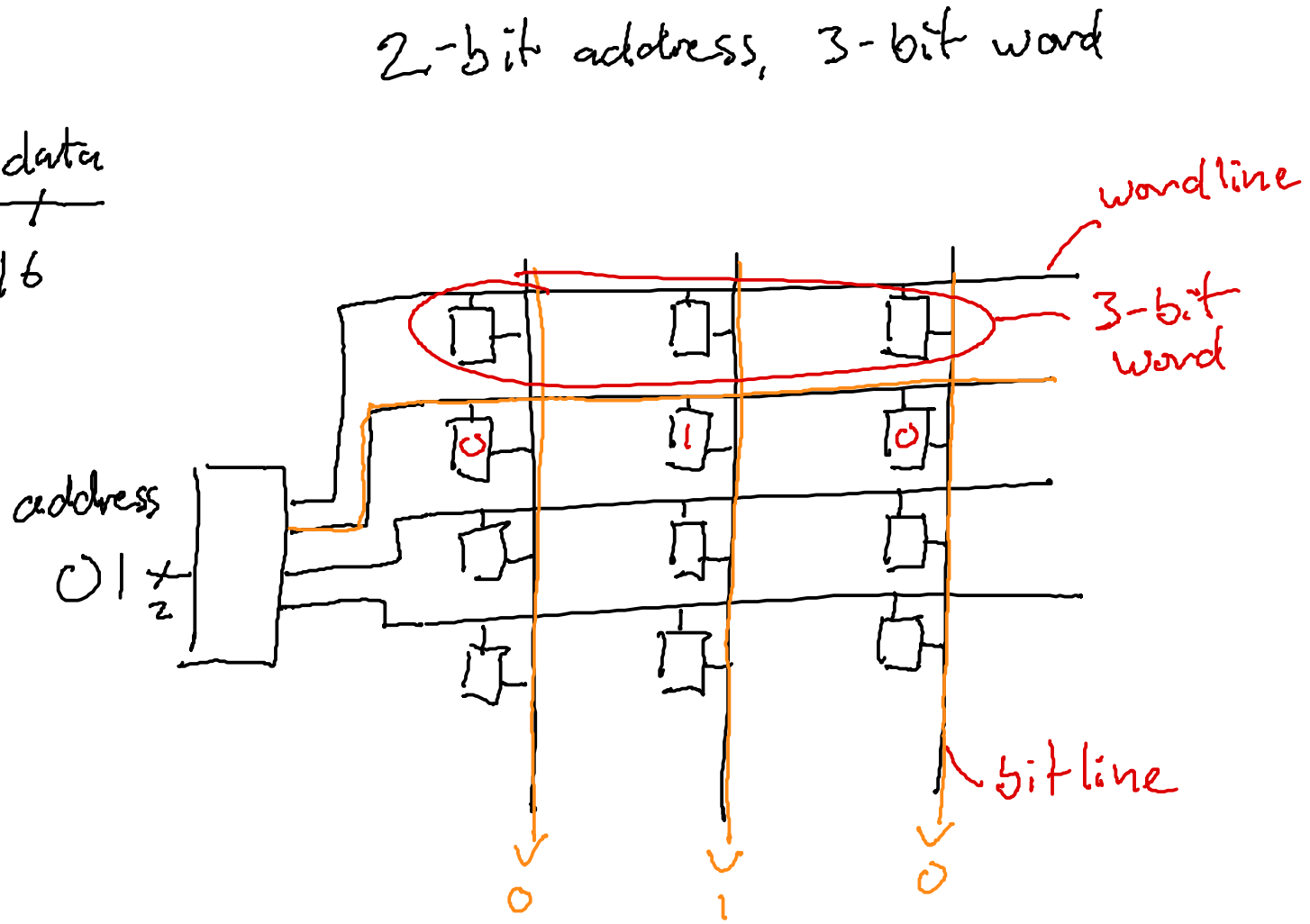
- Do modern computers use DRAM or SRAM or both?
- Will we be using memory arrays?
- Can we go over why learning about RAM and ROM is necessary for the class? This feels disconected from the other material.

By the end of class today, you should be able to

- Describe the tradeoffs in memory between speed, storage, access, energy, and cost.
- Describe where register files, caches, DRAM, Flash, and spinning hard drives fit in the tradeoff space
- Instantiate a ROM in the FPGA

Part 1: How is memory structured?





Part 1: How is memory structured?

Wordline activates a row (word) of the memory for reading/writing

Bitline connects to a column, and reads/writes an individual bit

Address specifies which word of memory to operate on

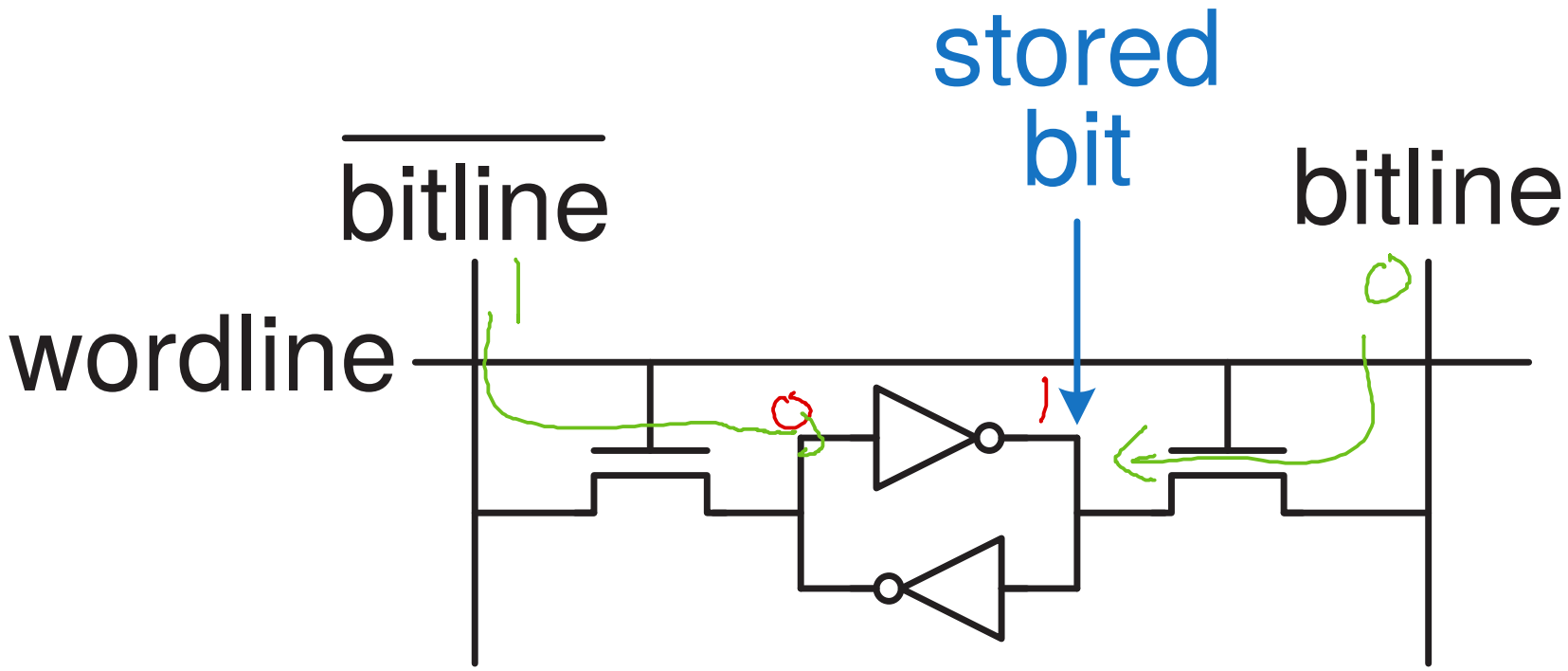
Decoder takes the address (as a binary number) and turns on the corresponding wordline

Data bus aggregates the bitlines to carry the complete word

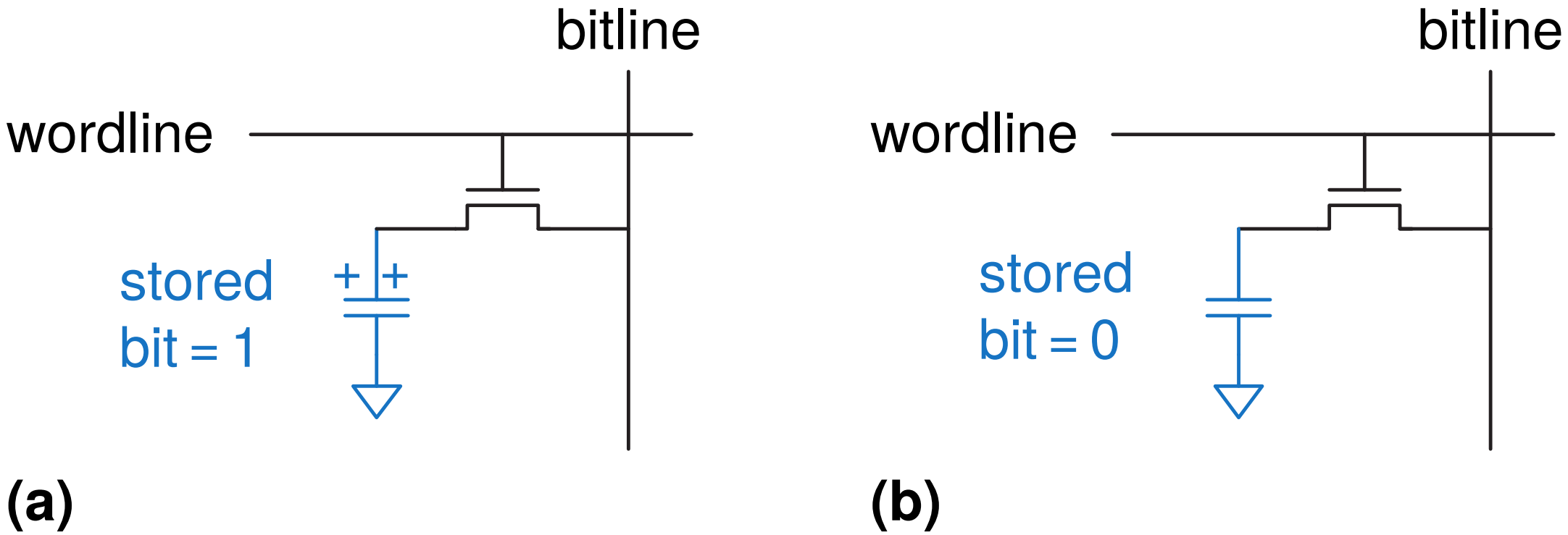
Part 2: Inside SRAM and DRAM

SRAM is "**static** random-access-memory"

DRAM is "**dynamic** random-access-memory"

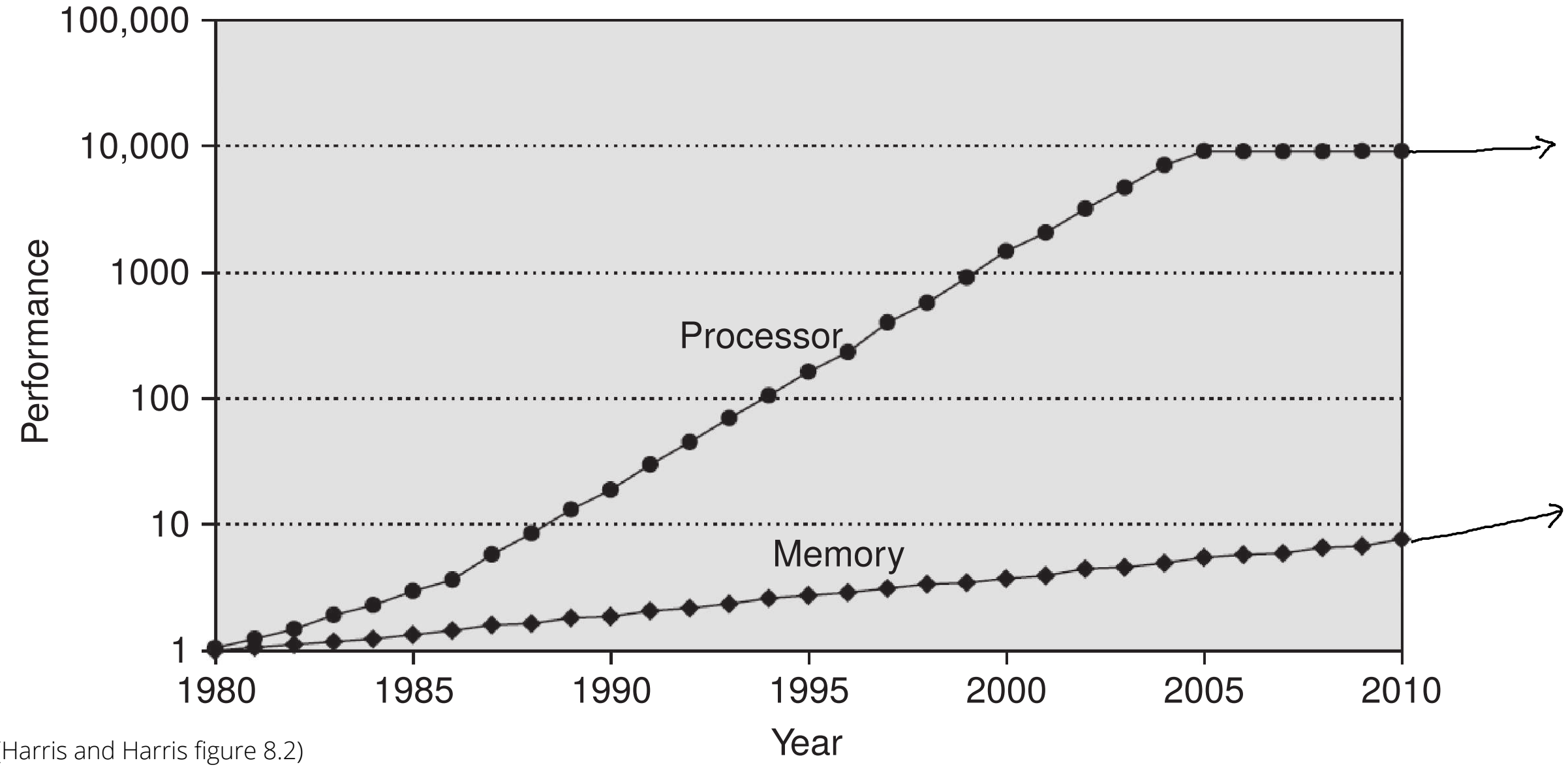

stored
bit
bitline
bitline
wordline

DRAM


bitline
wordline
stored
bit = 1
+
+
(a)
bitline
wordline
stored
bit = 0
(b)

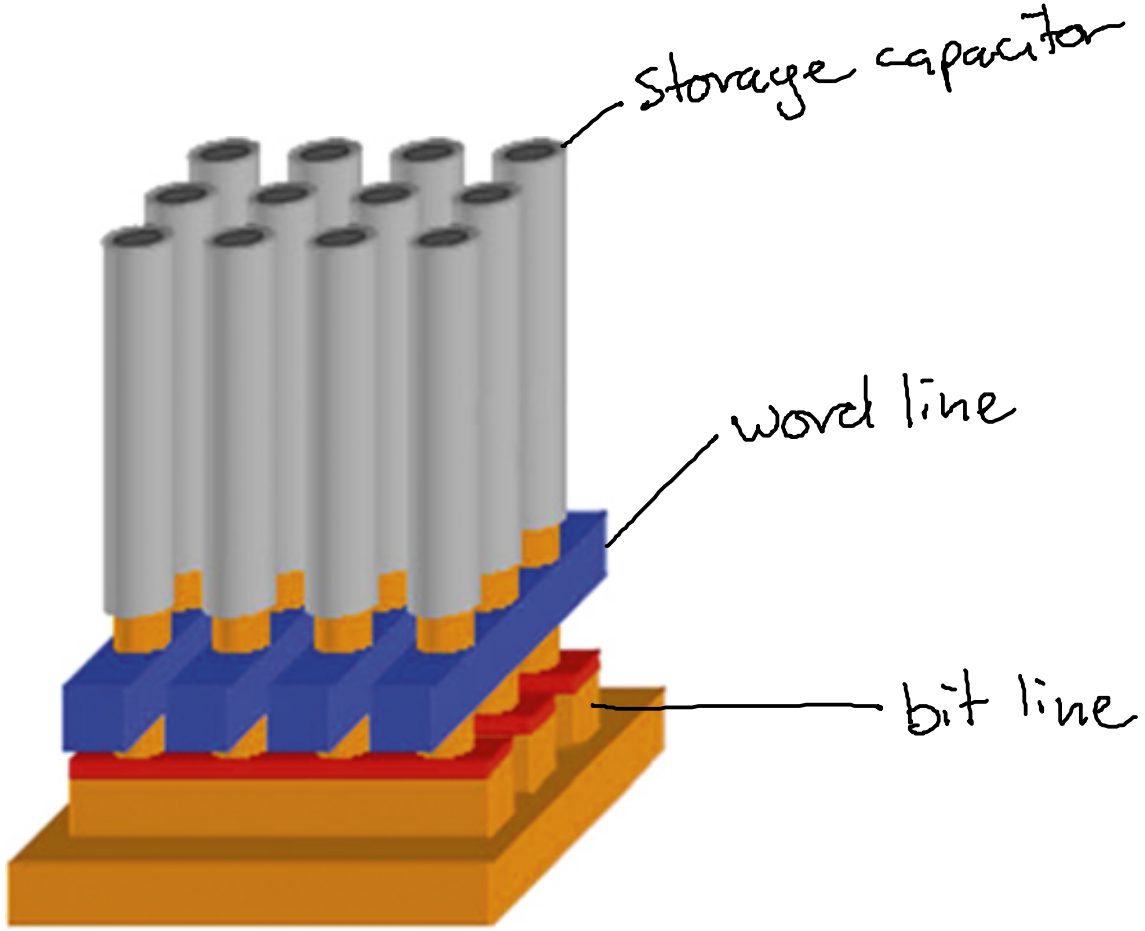
Part 3: Why do we need different kinds of memory?

Memory vs CPU speeds

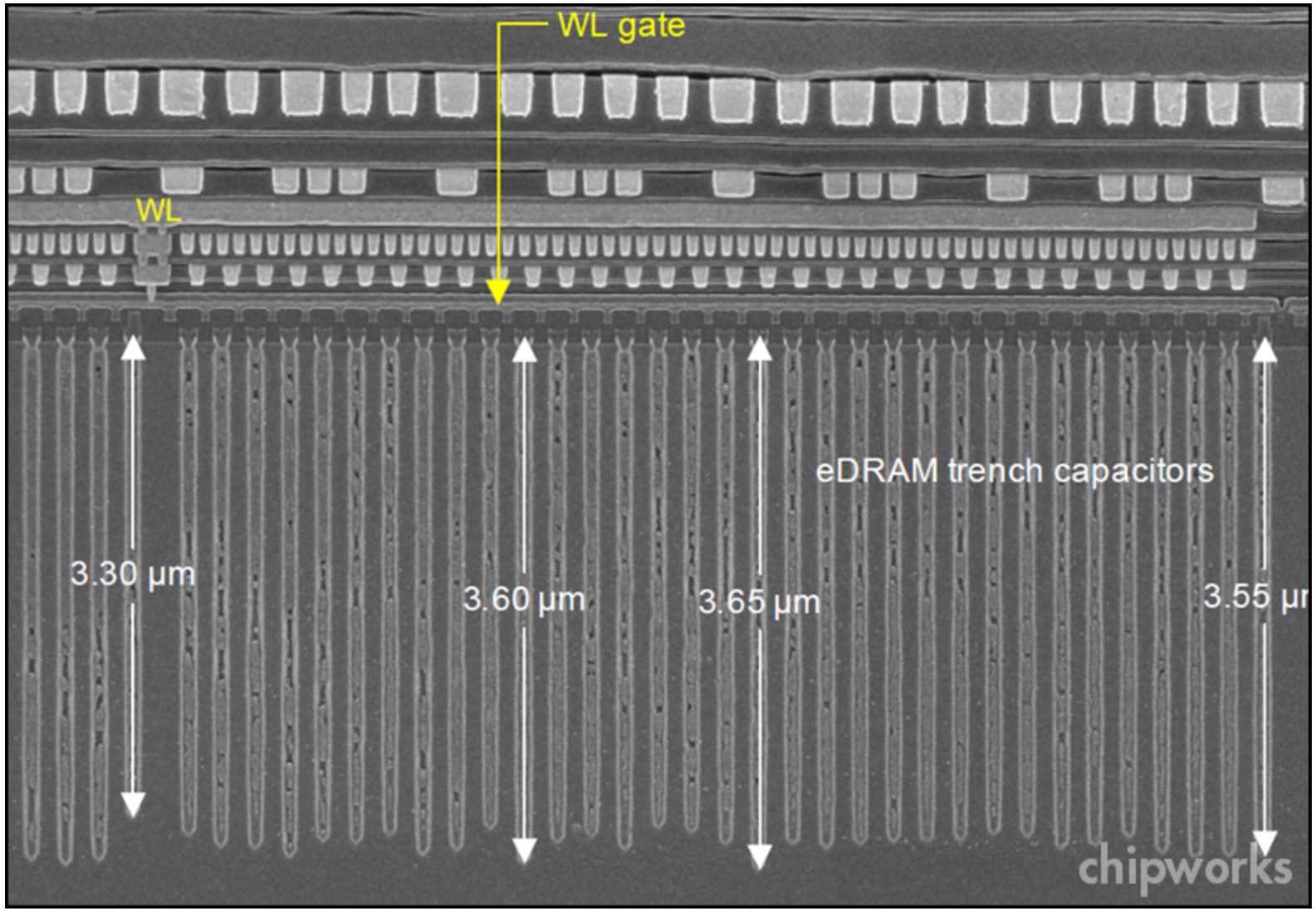


(Harris and Harris figure 8.2)

DRAM cell



DRAM



(image from chipworks http://chipworksrealchips.blogspot.com/2014/02/intels-e-dram-shows-up-in-wild.html)

Comparing memory technologies

	SRAM				
	Register file	Cache	DRAM	Flash	Spinning disk
Cost/bit	$$$$	$$$	$$	$	¢
Speed	1 clock cycle (1 ns)	10 cycles	100+ cycles	microseconds	milliseconds
Non-volatile	✗	✗	✗	✓	✓
Typical size	250 bytes	8 MB	8 GB	250 GB	6 TB

Memory in the FPGA

Just like a flip-flop: describe the behavior you want, and Radiant will "infer" the RAM/ROM for you.

Final project

Your project must:

1) take some sort of input,
2) compute on it, and
3) produce some sort of output

Hardware info and inspiration on the course website!

You also have the option to build an ARM CPU.

For Wednesday

1. Study for the exam!

2. Email me about your project team