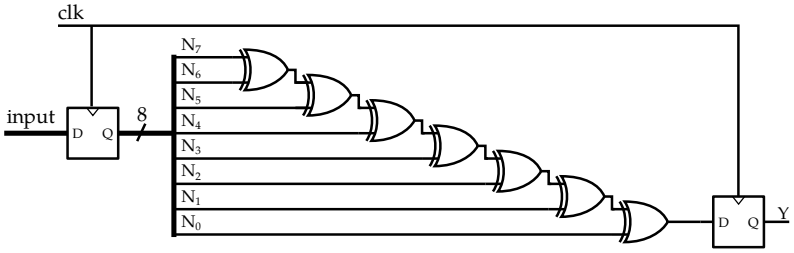
Sequential timing worksheet

ES 4, 7 November 2024

Gate	t_{pd} (ns)	t_{cd} (ns)
2-input XOR	5.0	1.7
clk-Q	1.5	0.75

DFF setup time 3.5 ns
DFF hold time 2.0 ns

What is the maximum clock speed this circuit can run at?



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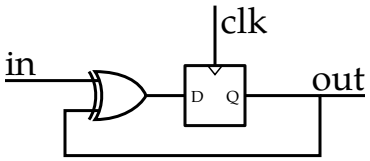

You would like to run this LFSR at 75 MHz. Will there be any setup time or hold time violations?