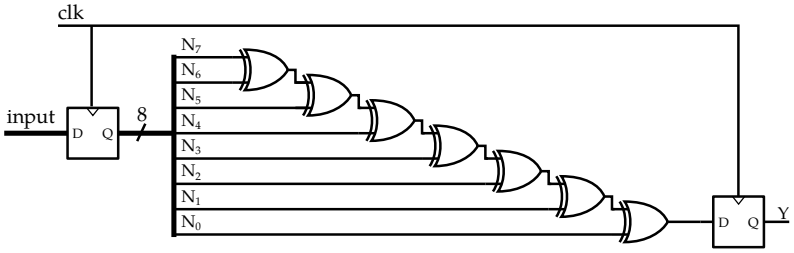
Sequential timing worksheet

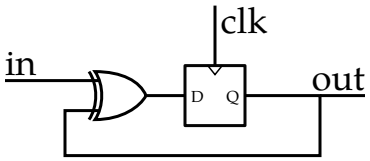
ES 4, 25 March 2019

Gate	t_{pd} (ns)	t_{cd} (ns)
2-input XOR	5.0	1.7
clk-Q	1.5	0.75
Setup time	3.5 ns	
Hold time	2.0 ns	

What is the maximum clock speed this circuit can run at?



What is the maximum clock speed this circuit can run at?



You would like to run this LFSR at 75 MHz. Will there be any setup time or hold time violations?