Course Overview: We will study in this course the basic principles of designing computers, register-transfer language and its application to computer design, basic computer organization, the central-processing unit, hard-wired and micro-programmed control units, Design of I/O interface, direct-memory access, interrupt, and I/O processor, Memory hierarchy, content-addressable memory, virtual memory, and memory management hardware, introduction to advanced topics in parallel computations, especially pipelining. The students will perform associated laboratory using Altera software and hardware. An assembler for MIPS will be implemented in the semester.


Prerequisites: EE 14 (Microprocessor Architecture and Applications) or Comp 40 (Computer Architecture and Assembly Language Programming).

Instructor: Professor Hwa Chang  
Office: Room 131, Halligan Hall; e-mail: hchang@eecs.tufts.edu; Telephone: (617) 627-5178  
Office hours:  
• Mondays: 2:50pm - 4:20 pm  
• Thursdays: 10:00am - 12:00pm  
• or by appointment

Teaching Assistant: Zhong Zou  
Office: 229A, Halligan Hall; e-mail: Zhong.Zou@tufts.edu; Phone: (617)820-6480  
Office hours: (Tentatively)  
• Tuesday: 10:00-11:00 am  
• Thursdays: 12:00pm - 1:00pm

E-mail List: We will have a class mailing list which will be frequently used to make announcements. Make sure you get on the mailing list!!

Course web page: All assignments, hints, handouts, and announcements will eventually be posted on the class' web page: http://www.eecs.tufts.edu/~hchang/ee126-f06 (tentatively).
**Homework:**

Weekly assignments to be completed by each student individually are due on Mondays at the beginning of class. Late homework will be penalized at 20% per day, and they will not be accepted after 5pm on Wednesdays. In case of illness, business travel or other good reasons, late homework will not be penalized, but they will not be accepted later than the following Monday. If you are turning homework late, please make sure the homework is stamped at the ECE main office, and placed in the TA's mailbox. For fully-credited late homework, you must have the instructor's PRIOR permission. You are encouraged to work on the homework with your classmates. However, avoid the suspicion of cheating and all homework has to be written up individually.

**Quizzes:**

There will be a quiz every Wednesday, if time allowed. The highest 7 grades will be used toward your final grade. Missed quizzes will not be re-taken. Quizzes will be given within the last 15 minutes of class covering previous material excluding the current lecture. Please plan on asking all questions ahead of time!!!

**Labs:**

There will be several labs consisting of tutorials and small designs. We will use a hardware description language, VHDL, to specify the design, and download the design to an Altera FPGA chip to validate it. No make-up of late labs are permitted. Some of the labs are demanding. Please plan your time accordingly. You will also design and implement an assembler for MIPS.

**Exams:** There will be one midterm exam on Monday Open Block, October 23 from 11:50 to 1:20pm and one two-hour accumulated final exam scheduled by the registrar on Friday, December 15 at 12:00pm-2:00pm. The exam times are fixed. Please plan accordingly. If for a good reason, you have to miss the exam, please give Professor Chang one week advance notice. If you miss the exam for an unexpected situation, e.g. sickness, accident, etc., you have to contact Professor Chang within 24 hours of the scheduled time.

**Attendance:** Although classroom attendance is not mandatory, it is highly recommended. Please note that you are responsible for all material covered in class, including changes in assignment due dates or exam schedules. Sometimes, some information is mentioned over email, but not in class or vice versa. Make sure you attend classes and keep track of your email!

**Course Grading:**

Homework 10%
Quizzes 15%
Labs 20%
Midterm 25%
Final 30%