

An SOI-Based Three-Dimensional Integrated Circuit Technology*

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Three-dimensional integrated circuits (3D-ICs) composed of active circuit layers that are vertically stacked and interconnected are expected to lead to improved logic devices, memories, CPU's, and photo sensors [1]. These circuits will require high-density vertical interconnections (3D vias) comparable in aspect ratio to present multilevel vias [2]. We have constructed and tested 3D ring oscillators and fully parallel 64x64 active pixel sensors using a 3D assembly technology which utilizes SOI wafers to achieve stacking of multiple circuit layers and unrestricted placement of dense 3D vias.

The construction of a 3D image sensor consists of bonding and interconnecting a SOI wafer with imaging circuits to a SOI wafer with pixel-parallel A/D converter circuits. The imager circuits were fabricated in a 10- μm epi layer on a 0.3- μm BESOI layer with a 1- μm BOX. The epi thickness was chosen to optimize optical performance in the visible spectrum. The A/D circuits were fabricated in a 1- μm SOI layer with a 1- μm BOX. Both wafers were processed with the same two-level metal 0.8- μm CMOS process designed to operate at 5 V. Prior to CMOS fabrication, silicon trenches were etched through the SOI layer of the A/D wafer and filled with TEOS oxide to form channels through which 3D vias would be etched to interconnect the two active layers. After wafer fabrication and test, the A/D wafer was inverted, aligned to the imager wafer, and bonded with a 3- μm adhesive. Then the bulk silicon was etched from the A/D wafer to expose the BOX. The BOX was used as a silicon etch stop to produce a thin uniform active layer and is an essential step in the 3D assembly technology. A set of shallow 3D vias was etched through the BOX, trench, and deposited oxides of the A/D wafer to expose metal pads on the first metal layer of the A/D wafer. A deep set of 3D vias was defined and etched entirely through the A/D wafer plus the adhesive to expose metal pads on the second metal layer of the imager wafer. The 3D vias were 6- μm square and were 2.7 and 7.5- μm deep for the shallow and deep vias, respectively. An aluminum alloy was deposited and defined to connect the metal pads of the two wafers.

These vias are illustrated in Fig. 1. The assembly was inverted and bonded to an oxidized silicon wafer for mechanical support, and the handle silicon was etched from the imager wafer to expose the epi layer for back side imaging. Bond pads were defined and etched through the BOX and 10- μm silicon to expose pads on the first metal layer of the imager. The assembly was diced into chips and packaged; then the characteristics of active pixel sensors, ring oscillators, and test structures were determined.

The resistances of shallow and deep via chains are shown in Fig. 2 along with the size of the 3D vias. The 10- μm square deep and shallow via resistances are comparable indicating that etching through the adhesive did not degrade the contact either by undercutting the adhesive bond or by contaminating the metal pad from adhesive residue. The increased resistance of the 6- μm deep vias is caused by a reduction of the via contact area due to shadowing during sputter cleaning. 3D ring oscillators were constructed by coupling an inverter from the imager wafer to an inverter in the A/D wafer with 6- μm 3D vias as shown in Fig. 3. The 3D oscillators were designed to test the 3D assembly process and were not laid out to optimize performance. 2D ring oscillators were also fabricated in the imager and A/D circuit wafers. The delays per stage of 3D ring oscillators are shown in Fig. 4 along with 2D oscillators from the imager wafer. The increased delay between the 2D and 3D oscillators is a result of the layout that tripled the parasitic capacitance between inverters and the 3D via resistance. The 3D ring oscillators were operated continuously for more than 120 days without degradation of the 3D vias. The 64x64 active pixel sensor coupled optical signals generated in N^+P diodes of the imager wafer to CMOS circuits in the A/D wafer by 6- μm deep vias. The A/D circuits periodically reset the potentials of the photodiodes and produced outputs proportional to the photodiode currents. The optical response of the active pixel sensor is shown in Fig. 5 in conditions of dim and bright illumination.

This work has shown the feasibility of stacking SOI circuits to build 3D-ICs. However, the size of the 3D vias must be reduced to build high performance systems. The via pitch will be limited by wafer-wafer alignment precision, the thickness of the bond layer, and the aspect ratio of trenches which can be lined with metal. The utilization of current wafer alignment equipment and low temperature oxide bonding will permit a significant reduction in 3D via size. Via density calculations as a function of alignment precision and aspect ratio are summarized in Fig. 6. The calculations assume three-level metal SOI circuits, 1- μm bond layers, fully landed 3D vias, and equal via space and size. The results indicate that a 5- μm minimum via pitch can be achieved with an aspect ratio of ten and an alignment precision of 1 μm , the capability of present wafer bonding equipment. The pitch decreases to 0.9 μm if the alignment capability of present steppers, 0.1- μm , is assumed along with recent advances in coating high aspect ratio trenches.

[1] Y. Akasaka, Proceedings of the IEEE Vol. 74, No. 12, December 1986
 [2] M. Reber and R. Tielert, IEEE Symposium on Circuits and Systems. Vol. 4, 1996

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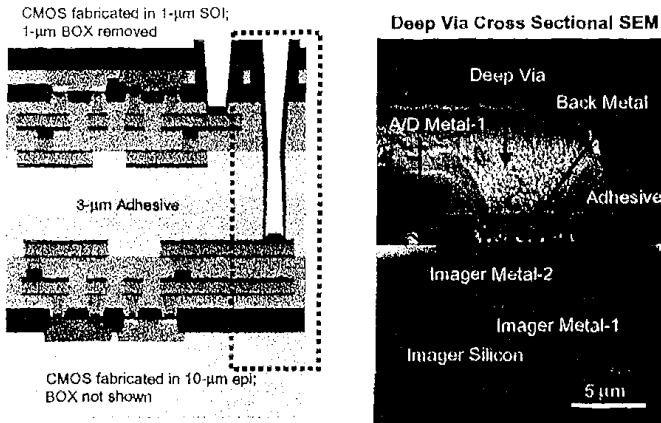


Fig. 1: Diagram of bonded A/D (top) and imager IC layers. An SEM of a deep 3D via is enclosed in the diagram.

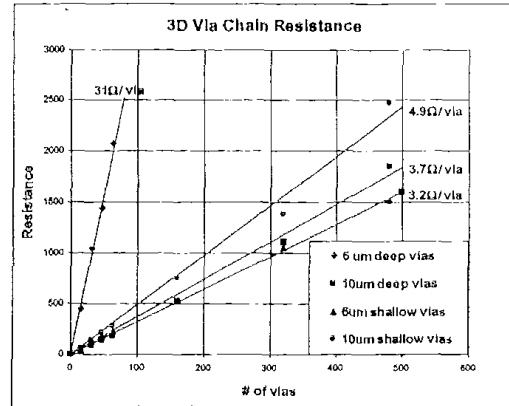


Fig. 2: Resistances of shallow and deep via chains.

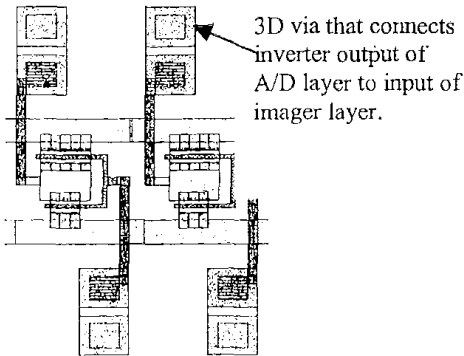


Fig. 3: Layout of the A/D layer of a 3D ring oscillator showing the pads used to connect the two active layers with 3D vias.

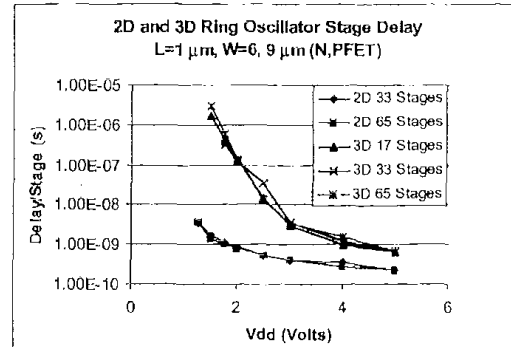


Fig. 4: Stage delays of 2D and 3D ring oscillators.

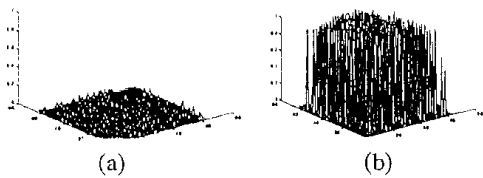


Fig. 5: Output of the 64x64 active pixel sensor in dim (a) and high (b) illumination conditions.

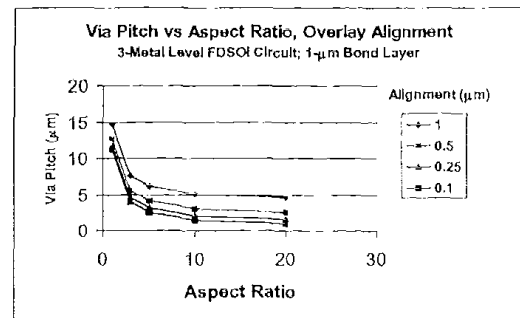


Fig. 6: Calculation of via pitch as a function of wafer-wafer alignment precision and aspect ratios of vias which can be metal coated.