2015 ES4 Introduction to Digital Logic Circuits

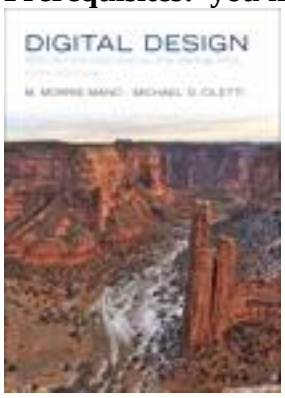
Class webpage: www.ece.tufts.edu/~karen/classes/ES4-1.html

A Link to the Trunk site will also be emailed to all enrolled students

Descriptions and Goals:

Welcome to the world of digital design. All aspects of digital system design and implementation methods will be investigated. To enforce the theoretical concepts, we will use VHDL/Verilog languages to model and simulate designs. Topics we will cover include number systems, codes and conversions. Two's complement representation. Boolean algebra and Karnaugh map minimization of Boolean expressions. We will then investigate logic gates and implement useful designs in the laboratory using SSI, MSI and LSI logic components. After covering combinational logic, we will introduce flip-flops, their characteristics and sequential circuit design including state machines. The course includes a **MANDATORY** hands-on laboratory, where every student will be actively involved and participating in design, simulation, implementation, reporting, writing and making oral presentations, as well as evaluating their teammates contributions and performance.

Prerequisites: you must have taken and passed ES3 Circuit Theory.



Textbook:

Digital Design, 5/E
M. Morris Mano
Michael D. Ciletti
ISBN-10: 0132774208 • ISBN-13: 9780132774208
©2013 • Prentice Hall • Cloth, 576 pp
Published 01/02/2012 • I

ES4 Workbook: You will receive a free copy of the ES4 workbook. Please pick a copy from the Halligan Hall ECE office. You should bring the notebook with you to each class.

References: Fundamentals of Digital Logic with VHDL Design, by Stephan Brown and Zvonko Vranesic. The publisher is McGraw Hill. , Introduction to Digital Logic Design", John Hayes, Addison Wesley, Reading, MA

Instructor: Dean Dr. Karen Panetta
Office: Room 236, Halligan Hall
Webpage: www.ece.tufts.edu/~karen
Email: karen@computer.org or Karen@ece.tufts.edu
Skype: Dr.KarenPanetta
Twitter: http://www.twitter.com/nerdgirlz
Facebook: http://www.facebook.com/people/Karen-Panetta/1283472323
SKYPE: Dr.KarenPanetta
Office Hours: Dean Panetta takes appointments for meetings with students.
Instructor: Dr. Denis Fermental, Assoc. Professor Emeritus.
Email: dfermental@ece.tufts.edu
Office Hours: TBD

Head Teaching Assistant: Ms. Wendy Wan, Mr. Jonathan Foley,
Emails:, Qianwen.Wan@tufts.edu, jonathan.foley@tufts.edu

Specific Topics:

1. Introduction to embedded system design of computers and applications.
2. Binary Systems, bits, base transformations (2 classes).
3. AND, OR, NOT functions, truth tables, gates. (2)
4. Alphanumeric codes, radix arithmetic.
5. 2's complement representation. (2)
6. Booelan theorems, algebraic simplification. (2)
7. Functions, complements, duals, canonical forms.(2)
8. Minterms, maxterms, Sum of Products, Product of Sums , (2)
9. NAND,NOR,XOR,XNOR gates, parity, gates with more than 2 inputs. (2)
10. Karnaugh Maps (3)
11. NAND, NOR implementations, bubble manipulations. (2)
12. Don't cares on K-maps, prime and essential prime implicants (2)
13. MSI combinatorial functions, multiplexor and decoders. (2)
14. Introduction to sequential circuits. (1)
15. SR, D, JK flip-flops, edge-triggered. (2)
16. Counter design using flip-flops.(1)
17. Moore and Mealy machines (3)

Assessment of accomplishments

- Mastering the material in this course is measured by:
- Quizzes
- Homework
- Laboratory sessions
- A midterm and final examination.

Each of these assessments is discussed in the following sections.

Quiz: There will be a quiz given every Wednesday. Two of the lowest quiz grades will be dropped. **No make-up quizzes will be given.**

Homework: There will be a homework assignment due every Wednesday at the **beginning** of class. Homework assignments are posted on the web and the front office. It is your responsibility to retrieve the homework assignment each week. Solutions to the homework will be placed in a book in the ECE office the day after the due date. All handouts given in class are also available in the ECE office.

No late homework will be accepted. If you cannot make class, turn in your homework in the front office and have it date stamped and put in the ES4 mailbox.

Collaboration is allowed and encouraged on homework. However, all students involved in collaboration must include the name of all collaborators at the top of their homework assignments. Failure to do so, will be considered plagiarism and will receive no credit.

Lab: There will be five labs consisting of design, hardwired implementation and Simulation. There will also be a final project. If a pre-lab is required for a lab, then the **Pre-lab will count** as a homework assignment that must be completed before you attend your scheduled lab section. Each student will conduct and individual lab and submit an individual lab report. If you need to attend a different lab section due to illness, you must pre-arrange a time with the Teaching Assistant. More information on lab requirements will be passed out next week. **YOU MUST PASS THE LAB COMPONENT OF THE COURSE with a 70% or better OR YOU WILL FAIL THE COURSE**.
All VHDL/Verilog program code and lab reports are to be the product of a single individual and not collaboration.
Students will sign up for a specific lab session. If you cannot make your scheduled lab session, you must inform the laboratory assistant to make-up a lab.
Please refer to the detailed laboratory guidelines for ES4.
The labs may also have an exit quiz that will count toward each lab report grade.

Examinations: There will be one hour-exam and one final exam. The midterm exam will be given in class on: **Wednesday, March 11, 2015**. The final exam will be announced according to the university schedule. If you have a schedule conflict for the hourly exam time for some unexpected reason, please get in touch with Dean Knox.

In Class attendance/presentation/professionalism:
5 additional bonus points will be added to the final exams of students who are present when randomly called upon anytime during the semester. If a student cannot make a class, professional courtesy requires a message to the instructor from a student indicating that they will not be present. You must maintain at least a 60% average in class homework quizzes and tests and a 70% average in lab work and projects.
Course Grading:
Homework Average: 10%

Project	10%
Quizzes	15%
Lab	25% (**must pass with a 70% or better**)
First hour-exam	20%
Final Exam	20%

Incomplete grades will not be given for failure to fulfill class requirements.