

EE126 Computer Architecture

Fall Semester 2014

www.ece.tufts.edu/~karen

In this course, students will study the basic principles of computer design, organization and performance. We will investigate how high level language programs are translated into the hardware and executed. We will study the interface between the software and hardware and what determines the performance of a program. Computer architecture techniques for improving both hardware and software performance will be investigated. Topics including data warehousing and energy efficiency will be covered along with a thorough understanding of parallelism, namely pipelining and the methods that must be employed to support parallelism. There will be laboratory exercises to model, simulate and evaluate the methodologies explored as well as implementing designs on an FPGA hardware device.

Textbooks: Computer Organization and Design: The Hardware/Software interface

References:

The Datacenter as a Computer: An Introduction to the Design of Warehouse-Scale Machines

Luiz André Barroso and Urs Hölzle

www.morganclaypool.com

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Pre-requisites: EE14: Microprocessor Architecture and Applications or Comp 40: Computer Architecture and Assembly Language Programming.

Class meeting time: Monday, Wednesday, 1:30-2:45pm, (G+ block) room Halligan 111B

It is expected that if you need to miss a class that you will email the professor before the class time.

Instructor: Dean Karen Panetta

Office: Room 236 Halligan Hall

Email: karen@ece.tufts.edu

Office Hours: regularly scheduled hours (TBD) and by appointment.

Lab Teaching Assistant: Wendy Wan **Email:** qianwen.wan@tufts.edu

Tentative Topics:

1. Introduction: Trends in computing
2. Performance metrics

3. Instruction sets: the Language of the computer
4. Model Abstraction and simulation. Introduction to FPGAs, and how to use them.
5. Addition and Subtraction hardware
6. Cascaded design in Verilog
7. Design of the Arithmetic Circuit: Carry Propagate adder design
8. Multiplier Algorithms
9. Datapath design
10. Pipelining
11. Hazards
12. Cache Design
13. Improving performance
14. Data warehousing
15. Energy efficiency

Quiz: There will be a quiz given every Monday, if time allows. The best 5 quizzes will be counted. No make-up quizzes will be given.

Homework: There will be a homework assignment due every Wednesday. Homework will be posted on the class web page. Solutions to the homework will be posted on the website. Any assignments or laboratory reports not handed in during class time, **MUST** be date stamped and turned in via email to the **TA**. **No late homework will be accepted.** Students are allowed and encouraged to collaborate on homework. However, all students will turn in the assignment and acknowledge their collaborators by name. Please keep copies of all your assignments and laboratories available.

Lab: There will be four labs consisting of design, modeling and Simulation and downloading to an FPGA. Any **Pre-labs will count** as a homework assignment. Each student will submit an individual lab report. All Lab reports will follow the posted lab write-up requirements posted on the ee126 web page. More information on lab requirements will be posted on the website. **Any programs, simulation code and laboratory reports are the work of the individual.**

Examinations: There will be a midterm and a final exam. The midterm exam will be given in class on: **October 15, 2014**. The final exam will be announced according to the university schedule. If you have a schedule conflict at any of the exam times for some unexpected reason, please get in touch with me as soon as possible.

Course Grading:

Homework Average:	10%
Quizzes	15%
Labs and oral Presentation	25%
Midterm -exam	25%
Final Exam	25%