4.27. Repeat Problem 4.26, for a *pnp* transistor.

4.28. Determine the region of operation for a room-temperature silicon *nnp* transistor that has \( \beta = 100 \) if (a) \( V_{CE} = 10 \text{ V} \) and \( I_B = 20 \mu \text{A} \); (b) \( I_C = I_B = 0 \); (c) \( V_{CE} = 3 \text{ V} \) and \( V_{BE} = 0.4 \text{ V} \); (d) \( I_C = 1 \text{ mA} \) and \( I_B = 50 \mu \text{A} \).

4.29. Determine the region of operation for a room-temperature silicon *pnp* transistor that has \( \beta = 100 \) if (a) \( V_{CE} = -5 \text{ V} \) and \( V_{BE} = -0.3 \text{ V} \); (b) \( I_C = 10 \text{ mA} \) and \( I_B = 1 \text{ mA} \); (c) \( I_B = 0.05 \text{ mA} \) and \( V_{CE} = -5 \text{ V} \).

**Section 4.5: Large-Signal DC Analysis of BJT Circuits**

4.30. Briefly discuss the procedure for performing a dc analysis of a BJT circuit using the large-signal circuit models.

4.31. Draw the fixed-base bias circuit. What is the principal reason that this circuit is unsuitable for the mass production of amplifier circuits?

4.32. Draw the four-resistor bias circuit for the BJT. Give the rule-of-thumb design guidelines for this circuit.

4.33. Use the large-signal models for the transistors illustrated in Figure 4.19 to find \( I_C \) and \( V_{CE} \) for the circuits of Figure P4.33. Assume that \( \beta = 100 \). Repeat for \( \beta = 300 \) and compare the results for both values.

**Figure P4.33**

4.34. Find \( I \) and \( V \) in the circuits shown in Figure P4.34. For all transistors, assume that \( \beta = 100 \) and \( |V_{BE}| = 0.7 \text{ V} \) in both the active and saturation regions. Repeat for \( \beta = 300 \).

**Figure P4.34**

4.35. Consider the circuit displayed in Figure P4.35. A Q-point value for \( I_C \) between a minimum of 4 mA and a maximum of 5 mA is required. Assume constant resistor values, and suppose that \( \beta \) ranges from 100 to 300. It is desired that \( R_B \) have the largest possible value while meeting the other constraints. Find the values of \( R_B \) and \( R_E \). The resistors in this problem are not required to be nominal values.

**Figure P4.35**

4.36. Consider the four-resistor bias network of Figure 4.28a with \( V_{CC} = 15 \text{ V} \), \( R_1 = 100 \text{ k} \), \( R_2 = 47 \text{ k} \), \( R_C = 4.7 \text{ k} \).
4.34. For \( R_E = 4.7 \Omega \). Suppose that \( \beta \) ranges from 50 to 200, \( V_{CC} = 0.7 \) V, and the resistors have a tolerance of \( \pm 5\% \). Find the maximum and minimum values of \( I_C \).

4.37. Consider the circuit shown in Figure P4.37. Find \( R_1 \) and \( R_E \). If a bias point of \( V_{BE} = 5 \) V and \( I_C = 2 \) mA is required. What are the closest 5%-tolerance nominal values for \( R_1 \) and \( R_E \)?

**Figure P4.37**

4.38. Find \( I_C \) and \( V_{BE} \) in the circuit of Figure P4.38.

**Figure P4.38**

4.39. Four-resistor bias circuit design. Suppose that \( V_{CC} = 20 \) V, \( R_C = 1 \) k\( \Omega \), and a \( Q \)-point of \( I_C \approx 5 \) mA is desired. The transistor has \( \beta \) ranging from 50 to 150. Design a four-resistor bias circuit. Use standard 5%-tolerance resistor values. Many correct answers exist for this problem. Design so that approximately one-third of the supply voltage is dropped across \( R_C \), one-third across the transistor (\( V_{CE} \)), and one-third across \( R_E \).

**Section 4.6: Small-Signal Equivalent Circuits**

4.40. Draw two small-signal equivalent circuits for the BJT.

4.41. Give the formulas for determining \( r_i \) and \( g_m \), assuming that \( \beta \) and the \( Q \)-point are known.

4.42. A certain npn silicon transistor at room temperature has \( \beta = 100 \). Find the corresponding values of \( g_m \) and \( r_i \) if \( I_C = 1 \) mA, 0.1 mA, and 1 \( \mu \)A. Assume that the device is operating in the active region.

**Section 4.7: The Common-Emitter Amplifier**

4.43. Why are coupling capacitors often used to connect the signal source and the load to discrete amplifier circuits? Should coupling capacitors be used if it is necessary to amplify dc signals? Explain.

4.44. Draw the circuit diagram of a common-emitter amplifier circuit that uses the four-resistor biasing network. Include a signal source and a load resistance.

4.45. Consider the common-emitter amplifier of Figure P4.45. Draw the dc circuit and find \( I_C \). Find the value of \( r_i \). Then calculate values for \( A_v \), \( A_{oG} \), \( Z_{in} \), \( A_i \), \( G \), and \( Z_0 \). Assume that the circuit is operating in the midband region for which the coupling and bypass capacitors are short circuits.

**Figure P4.45**

4.46. Repeat Problem 4.45 if all resistance values, including \( R_i \) and \( R_L \), are increased in value by a factor of 100. If you have also worked Problem 4.45, prepare a table comparing the results for the low-impedance amplifier with those for the high-impedance amplifier. (Comment: When we consider the high-frequency response of these circuits, we will find that the gain of the high-impedance circuit falls off at lower frequencies than the gain of the low-impedance circuit. Thus, if we want constant gain to extend to very high frequencies, we should use the low-impedance circuit.)

**Section 4.8: The Emitter Follower**

4.47. Draw the circuit diagram of a discrete emitter follower.

4.48. For a small-signal midband analysis of an amplifier, with what do we replace the coupling capacitors? Do voltage sources? Do current sources? Very large inductors?
4.49. Draw the small-signal equivalent circuits for the circuits illustrated in Figure P4.49.

(a) Common-emitter amplifier with unbypassed emitter resistor

(b) Variation of the emitter follower using a dc current source for biasing

(c) Variation of the common-base amplifier (assume that the radio-frequency choke (RFC) is an open circuit for the ac signals)

Figure P4.49 Amplifier circuits.

4.50. Briefly describe the small-signal analysis procedure for finding the output resistance of an amplifier.

4.51. Consider the emitter-follower amplifier of Figure P4.51.
Draw the dc circuit and find $I_{CQ}$. Find the value of $r_e$. Then calculate midband values for $A_v$, $A_{vo}$, $Z_{in}$, $A_i$, $G$, and $Z_o$.

4.52. Repeat Problem 4.51 if all resistance values, including $R_1$ and $R_L$, are increased in value by a factor of 100. Prepare a table comparing the results for the low-impedance amplifier with those for the high-impedance amplifier.

4.53. Draw the small-signal equivalent circuit for the amplifier shown in Figure P4.53. Derive expressions for the voltage gain and input impedance in terms of the resistor values, $r_e$, and $\beta$. Assume that the capacitors are short circuits for the signals.

4.54. Find the values of $I_{CQ}$, $r_e$, $A_v$, and $Z_{in}$ for the circuit of Problem 4.53 if $V_{CC} = 15\ \text{V}$, $\beta = 100$, $V_{BEQ} = 0.7\ \text{V}$, $R_B = 270\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, $R_E = 100\ \Omega$, and $R_L = 1\ \text{k}\Omega$. Repeat for $R_E = 0$ and prepare a table comparing the results.

4.55. Find an expression for the output impedance of the amplifier displayed in Figure P4.53.

4.56. Draw the small-signal equivalent circuit of the circuit shown in Figure P4.56, and derive expressions for the input impedance and voltage gain. Assume that the capacitors are short circuits for the signals.
Consider the common-emitter amplifier illustrated in Figure P4.59. The ac source in series with the dc supply represents power-supply hum. (a) Assume that a large bypass capacitance is connected between points A and E. Draw the small-signal equivalent circuit, including the hum source. Solve for $A_{\text{hum}} = v_o / v_{\text{hum}}$, assuming that $v_i = 0$.

(b) Now consider connecting the emitter bypass capacitor from point E to ground, and again find $A_{\text{hum}}$. Notice that if $v_{\text{hum}} = 0$, the two equivalent circuits are identical, so they perform equally as far as the source signal $v_i$ is concerned. Which option is best for the connection of the bypass capacitor? Why?

Consider the circuit of Figure P4.56 with $V_{CC} = 15$ V, $R_1 = 10$ kΩ, $R_2 = 10$ kΩ, $R_B = 100$ kΩ, $R_E = 10$ kΩ, and $R_L = 4.7$ kΩ. Assume a transistor having $\beta = 200$ and $V_{BEQ} = 0.7$ V. Evaluate the expressions found in Problem 4.56 for input impedance and voltage gain.

Consider the common-emitter amplifier circuits displayed in Figure P4.58. The ac sources shown in series with the dc supply sources represent power-supply hum. Draw the small-signal equivalent circuits. Be sure to include the hum source in your model. Notice that if $v_{\text{hum}} = 0$, the two equivalent circuits are identical. Find an expression for the voltage gain $v_o / v_{\text{in}}$ if $v_{\text{hum}} = 0$. Then set $v_{\text{in}} = 0$ and solve for $A_{\text{hum}} = v_o / v_{\text{hum}}$ for each circuit. Evaluate the gain values for $V_{CC} = 15$ V, $V_{BEQ} = 0.7$ V, $\beta = 100$, $R_B = 1$ MΩ, and $R_C = 4.7$ kΩ. Which of these circuits is preferable? Why?

Find the value of $V_{CEQ}$ for the circuit of Figure P4.60. Draw the small-signal equivalent circuit and find an expression for the small-signal output impedance $Z_o$ in terms of $\beta$, $r_e$, $R_1$, and $R_2$. Evaluate $Z_o$ for the values shown in the figure.
4.61. Consider the voltage-reference circuits illustrated in Figure P4.61. The dynamic small-signal resistance of each Zener diode is $r_D = 100 \, \Omega$. Find the dc output voltage of each circuit. Draw the small-signal equivalent circuit, and derive an expression for the output impedance of each circuit. Evaluate the expressions for the resistances and transistor parameters shown.

**Figure P4.61**

**Section 4.9: The BJT as a Digital Logic Switch**

4.62. Draw the circuit diagram of an RTL inverter. In what region is the transistor intended to operate if the input is high? Low?

4.63. Draw the circuit diagram of an RTL NOR gate.

4.64. Consider the transfer characteristic of the RTL inverter shown in Figure 4.43. Sketch the transfer characteristic to scale for the values shown in Figure P4.64. Sketch the output voltage $v_o(t)$ to scale versus time if (a) $v_{in}(t) = 2.7 \sin(2000\pi t)$; (b) $v_{in}(t) = 2.7 + \sin(2000\pi t)$; (c) $v_{in}(t) = 2.7 + 5 \sin(2000\pi t)$.

4.65. Consider the RTL inverter of Figure P4.64. Assuming that we require the minimum output voltage with the transistor in the cutoff region to be $V_{OH} = 6 \, \text{V}$, what is the maximum number of driven gates (i.e., the fan-out) that can be connected? Assume that the driven gates have input circuits identical to those of the RTL inverter.

4.66. If $V_{in} = 6 \, \text{V}$ for the circuit of Figure P4.64, find the minimum value of $\beta$ to ensure that the transistor is in saturation.

4.67. If $V_{OL}$ (i.e., the output voltage in the low logic state) is required to be less than 0.5 V for the circuit of Figure P4.54, what is the maximum fan-out allowed (i.e., the maximum number of inputs that can be connected) if the driven gates are also RTL circuits?