Lecture #36: Output Stages

Output Stage Requirements

* Low Output Impedance: Needs to drive low-value output loads.

* Large output signal swing: Since this is the last stage, the maximum voltage swing appears in this stage.

* Power delivering capacity: Since the load is small & the signal swing is large, the power delivered to the load must be done efficiently.

* High Input Impedance: So not to reduce the gain of the previous stage.

Let's look at the most simple of output stages i.e. emitter-follower configuration.
Emitter Follower as an output stage.

![Circuit Diagram]

Figure 36.1

* We know the small-signal gain for the emitter follower is close to unity.
Since this is going to be used as an output stage, let’s look at the large signal analysis of input vs. output.

Consider Figure 36.1, we can write

\[ V_o = V_i - V_{BE1} \quad (36.1) \]

Since

\[ I_C1 = I_{bias} + I_L = I_{bias} + V_o / R_L \]

\[ \hat{o} \quad V_{BE1} \text{ is not constant.} \quad (36.2) \]
\[ V_{BE1} = \frac{kT}{q} \cdot \ln \left( \frac{I_C}{I_S} \right) - (35.3) \]

\[ V_o = V_i - V_T \cdot \ln \left( \frac{I_{bias} + V_o/R_L}{I_S} \right) - (35.4) \]

The above equation shows the non-linear relation between \( V_o \), \( V_i \).

* Since the non-linear term is a natural log. of the change in load current, this change in \( V_{BE} \) is very small.

Eg. A change of load current from 1mA to 30mA results in \( \Delta V_{BE} \geq 90mV \)

* Moreover, since this power amplifier is preceded with a lot of gain, the input referred non-ideality is very minute.

* Therefore, assuming \( \Delta V_{BE} \) is very small, let's draw the input-output characteristics.
Figure 36.2: Transfer characteristic of emitter follower for low(RL2) & a high(RL1) value of load resistance.

* Since we assumed the $V_{BE1}$ to be almost constant, the $V_o - V_i$ relation is a linear one with a $V_{BE1}$ offset.

* When $V_i$ is made and large and positive, the output clips when $Q_1$ saturates i.e.
  $V_o = V_{cc} - V_{CE1(sat)}$

* When $V_i$ is negative, the clipping depends on the load.
  - When the load is large ($RL1$)
    $\frac{V_{cc}}{RL} < I_{bias}$
then $V_o = -V_{EE} + I_{bias}(sat)$

where, $I_{bias}(sat)$ is when the transistor in the current source goes into saturation.

- When the load is small i.e.
  $\frac{V_o}{R_L} > I_{bias}$

  the output clips at
  $V_o = -I_{bias} \cdot R_L$

  since $I_{cl} = 0$ or $Q_4$ is cut-offs.

Therefore, if the output signal exceeds the clipping point then the output distorts.
Power Efficiency:

* One of the key figures-of-merit in an output stage is how efficiently the power is delivered to the load.

* Before we calculate efficiency, let's look briefly at some power calculation techniques.

* The instantaneous power in any element is given by:

\[ P_i(t) = v_i(t) \cdot i_i(t) \]

where, \( v_i(t) \rightarrow \) instantaneous voltage across element

\( i_i(t) \rightarrow \) current through the element

* If we assume a sinusoidal excitation, the average power is given by:

\[ P_{avg.} = \frac{1}{T} \int_0^T v_i(t) \cdot i_i(t) \cdot dt \]

where, \( T \rightarrow \) time period of the sine wave.
**Example 1**

\[ i(t) = i_{bias} + I_{pk} \cdot \sin wt \]

\[ P_{avg} = \frac{1}{T} \int_0^T i(t) \cdot V_{cc} \, dt = \frac{V_{cc}}{T} \int_0^T i(t) \, dt \]

\[ = \frac{V_{cc}}{T} \left[ \int_0^T i_{bias} \, dt + \int_0^T I_{pk} \cdot \sin wt \, dt \right] \quad \left[ \text{average of } \right] \]

\[ = \frac{V_{cc}}{T} \cdot i_{bias} \left[ T - 0 \right] = \frac{V_{cc} \cdot i_{bias}}{T} = P_{avg} \]

**Example 2**

\[ V(t) = V_{pk} \cdot \sin wt \]

\[ P_{avg} = \frac{1}{T} \int_0^T i(t) \cdot V(t) \, dt \]

or, \[ P_{avg} = \frac{1}{T} \int_0^T V_{pk} \cdot \sin wt \cdot \frac{i(t)}{V_{pk}} \cdot \sin wt \, dt \]

\[ = \frac{V_{pk}^2}{R \cdot T} \int_0^T \sin^2 wt \, dt = \frac{V_{pk}^2}{R \cdot T} \int_0^T \left( \frac{1}{2} - \frac{1}{2} \cos 2wt \right) \, dt \]

\[ = \frac{V_{pk}^2}{2 \cdot R \cdot T} \left[ T - 0 \right] = \frac{V_{pk}^2}{2 \cdot R} \]

\[ P_{avg} = \frac{(V_{pk}/V_2)^2}{R} \quad \frac{V_{pk}}{V_2} \rightarrow \text{Root-mean-square (RMS) value of } V(t). \]
Efficiency:

Efficiency of an power amplifier indicates the useful power delivered to the output load compared to the total power delivered or dissipated consumed in the power supply.

It can be defined as:

\[ \eta = \frac{P_o}{P_{\text{supply}}} \times 100\% \]

where, \( P_o \rightarrow \) power delivered to the load
\( P_{\text{supply}} \rightarrow \) power consumed from the supply.

\( x \) The power which is not delivered to the load, is dissipated in the output stage.

\( x \) Let’s look at an example.

Example 10.5 pg-684 from text book
Example 10.5 pg-684

1. \[ P_L = \left( \frac{V_{pk}}{\sqrt{2}} \right)^2 \times \frac{1}{R_L} = 10 \text{W} \]

   \[ \Rightarrow V_{pk} = \sqrt{10 \times 8 \times 2} = 12.65 \text{V} \]

2. \[ V_{cc} = V_{pk} + V_{CEO(sat)} = 12.65 + 0.2 = 12.85 \text{V} \]

3. \[ V_{ee} = -12.85 \text{V} \]

4. In order for \( V_0 \) not to clip for \( V_0 > -V_{ee} \)

   \[ I_{bias} \times R_L = \left| V_{ee} \right| - V_{CEO(sat)} \Rightarrow I_{bias} = \frac{12.65}{8.52} \approx 1.6 \text{A} \]

   \[ I_{bias} = 1.6 \text{A} \]

5. \[ P_{Vcc} = V_{cc} \times I_{Q\ \text{avg}} = V_{cc} \times I_{bias} = 12.85 \times 1.6 \]

   \[ = 20.56 \text{W} \]

   \[ P_{Vee} = V_{ee} \times I_{bias} = 20.56 \text{W} \]
6 Efficiency

\[ \eta = \frac{P_L}{P_{\text{Vcc}} + P_{\text{VEE}}} \times 100\% = \frac{10}{2 \times 20.56} \times 100 = 24.13\% \]

\[ \eta \geq 25\% \]

7 Power dissipated in \textit{I_{bias}}

\[ P_{\text{bias}} = |V_{\text{EE}}| \cdot I_{\text{bias}} = 20.56 \, \text{W} \]

8 Total power consumed from the supplies (\text{Vcc} and \text{VEE}) should be equal to the total power dissipated by the output stage & load. \textit{IR}.

\[ P_{\text{Vcc}} + P_{\text{VEE}} = P_L + P_{\text{bias}} + P_{Q1} \]

\[ \Rightarrow P_{Q1} = (P_{\text{Vcc}} + P_{\text{VEE}}) - (P_L + P_{\text{bias}}) \]

\[ = 2 \times 20.56 \, \text{W} - (10 + 20.56 \, \text{W}) \]

\[ = 10.56 \, \text{W} \]

8.2