

# Development of a CMOS 310Mb/s receiver for free space optical wireless links

Vinod A. Lalithambika, Valencia M. Joyner, David M. Holburn and Robert J. Mears

Department of Engineering, University of Cambridge, Cambridge CB2 1PZ, United Kingdom

## ABSTRACT

This paper presents the design and implementation of a CMOS 310Mb/s receiver for use in a multi-channel 155Mb/s Manchester-coded optical wireless link. The receiver consists of a pre-amplifier followed by a post amplifier circuit. The pre-amplifier is a three stage transimpedance amplifier with an NMOS load at the output of each stage to control gain and stability. To allow the sensitivity of the performance to key parameters to be visualized a nomograph technique was developed. The contours of the nomograph show how DC bias, dominant pole frequency and the gain of each stage vary with transistor dimensions. This allows the designer to select transistor sizes for a given bit rate and for stable operation. The design has been optimized to achieve -30dBm sensitivity at a BER of  $10^{-9}$ .

The post amplifier consists of a differential amplifier followed by a chain of inverters with feedback and produces rail-to-rail output swing. The design utilizes a replica biasing circuit which automatically biases the first amplification stage and provides an intrinsic high pass transfer function to attenuate 1/f receiver noise. The need for external filtering for the receiver is eliminated by this feature.

The design is being realized in a 0.7 micron commodity mixed signal CMOS process by Alcatel Microelectronics.

**Keywords:** CMOS Analog Integrated Circuits, Optical Receivers, Optical Wireless Communication, Transimpedance Amplifier.

## 1. INTRODUCTION

The era of data, voice, and video-on-demand is rapidly emerging. Mobile communications devices with intensive computation capabilities, such as laptops, personal digital assistants (PDA), and cellular phones have increased in popularity at enormous rates. Gartner Group, an independent research and analysis group on information technology industries, estimates that there will be roughly 1 billion mobile devices on the market by 2003 and by this time, 40 percent of all business to consumer e-commerce will be conducted via mobile devices. The stimulation of growth in the wireless local area network (WLAN) industry has been catalyzed by this intense drive for mobility by users. WLANs are expected to revolutionize indoor mobile computing by providing cable-free access to data and communications services to mobile users, and facilitating network upgrading and reconfiguration with minimal cost. One of the greatest challenges in WLAN development is the provision of systems achieving high bandwidths comparable to wired networks. Current wireless interfaces are available, but offer data rates suitable only for textual email and small file transfer.

There are two primary media available for wireless networking: radio frequency (RF) and optical systems. RF based systems are the dominant technology in the industry at present. Wide area coverage without the obstruction of communication by physical barriers can be provided with RF based systems, but data rate limitations, due to RF spectrum regulation, are a drawback to this approach. RF spectrum licencing, varying across the globe, adds an additional constraint to wireless networking and greatly affects future development. The Bluetooth wireless technology is currently being developed through the collaboration of computing and communications industry leaders establishing a common set of standards for linking mobile devices over short ranges. This RF standard is a potentially low cost approach without the need for frequency licensing, but with data rates of less than 1MHz. High frequency RF systems are inherently more costly and suffer from high power consumption. Optical systems have the potential to provide low cost, and low power wireless networking solutions offering unregulated bandwidths in the THz range. Optical networks will eliminate bottlenecks in connecting wireless LANs to high speed Ethernet backbone networks, and thus create a seamless network.

---

Send correspondence to Vinod A Lalithambika E-mail: va211@eng.cam.ac.uk

The challenge is to develop an integrated transceiver for high speed free space communication within a building. The search for a suitable transceiver should address the requirements of full integration, sensitivity, low power dissipation, eye safety and high bit rate.

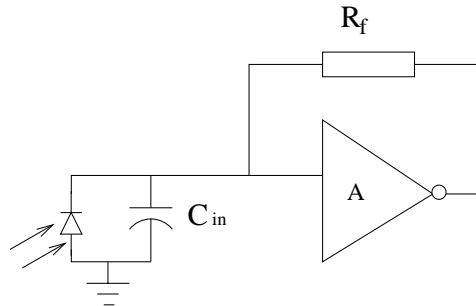
The optical receiver presented in this paper consists of two major stages of which the first is a transimpedance amplifier as described in Section 2. The second stage is a post amplifier circuit and is described in Section 3. Section 4 presents the realization of the complete receiver circuit including layout considerations. Simulated results are shown in Section 5.

## 2. THE TRANSIMPEDANCE AMPLIFIER

Optical wireless receivers employ a transimpedance design<sup>1-3</sup> because it offers a good compromise between bandwidth and noise, both of which are influenced by the capacitance of the photodiode. Because optical wireless receivers must use photodiodes with significant area, a design optimized for high input capacitance is required.

### 2.1. The full CMOS transimpedance amplifier

The transimpedance amplifier with open loop gain  $A$  can be represented by a voltage amplifier with resistive feedback (Figure 1).

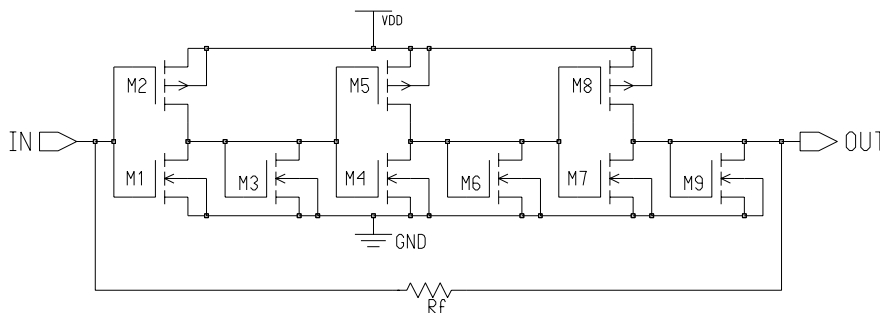


**Figure 1.** Transimpedance amplifier: Block diagram

The input capacitance is large as it includes the photodiode capacitance (typically 2-10pF). The dominant pole of this structure is at the input node and is given by

$$BW = \frac{1 + A}{2\pi R_f C_{in}} \quad (1)$$

For a given transimpedance,  $R_f$ , high bandwidth requires high gain,  $A$ , or for a given bandwidth,  $BW$ , high resistance



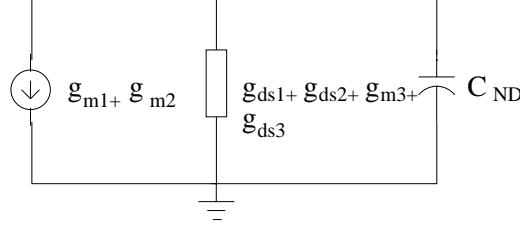
**Figure 2.** The preamplifier

requires high gain. For a given amplifier bandwidth the resistance should be maximal and vice versa. In addition,

the gain  $A$  should be maximised. However, the maximum achievable gain is limited by stability requirements. An increased gain shifts the higher order poles of the amplifier down and thus reduces the phase margin. To obtain a stable structure, the maximum open loop gain,  $A$ , is limited. However, the transimpedance can be adjusted to obtain the necessary bandwidth.

The circuit topology<sup>4</sup> is as shown in Figure 2. Each stage consists of a CMOS inverting amplifier with a diode-connected NMOS load. The advantage of this circuit is that it does not require any additional biasing circuitry.

## 2.2. Design equations



**Figure 3.** The model of output port of single stage

The 3-identical-stage amplifier is designed with a -3dB bandwidth of 217MHz. The principal stability requirement is that the voltage amplifier pole frequencies be above the receiver bandwidth so that the phase shift in the voltage gain,  $A$ , is less than  $45^\circ$  over the receiver bandwidth. In practice the phase shift in  $A$  should remain less than  $45^\circ$  as the frequency is increased, until the feedback carries the loop voltage gain below unity. Mathematically, this unity loop frequency works out to be equal to the photocurrent-to-output-voltage response pole frequency, or receiver bandwidth; thus, the stability requirement is that the phase shift in the forward voltage gain,  $A$ , be less than  $45^\circ$  over the receiver bandwidth. The out-of-band rolloff is not important because the out-of-band voltage loop gain is less than unity. To achieve sufficient phase margin, the bandwidth of each stage ( $BW_1$ ) is designed to be 939.93MHz. This corresponds to a phase shift of  $13^\circ$  per stage at the  $-3dB$  bandwidth ( $BW = 217MHz$ ). As the bandwidth of the transimpedance amplifier (Equation 1) and thus the stability of the system is directly related to gain,  $A$ , and as  $A$  depends now on the third power on the amplification ( $A_1$ ) of a single stage, its value should be strictly controlled.

Consider the model of the output port of a single stage (Figure 3). The DC gain of this single stage is given by:

$$A_1 = \frac{g_{m1} + g_{m2}}{g_{m3} + g_{ds1} + g_{ds2} + g_{ds3}} \quad (2)$$

To analyse the topology, two  $W/L$  ratios are defined:

$$X(1) = \frac{(W/L)_{M1}}{(W/L)_{M3}} \quad X(2) = \frac{(W/L)_{M2}}{(W/L)_{M3}} \quad (3)$$

As the amplifier has DC negative feedback, the output voltage has to be equal to the input voltage, so that  $(V_{GS} - V_{tn})$  of all NMOS transistors are equal. Both  $g_m$  and  $g_{ds}$  are functions of  $X(1)$  and  $X(2)$ . Hence

$$A_1 = \frac{f_1(X(1), X(2))}{f_2(X(1), X(2))} \quad (4)$$

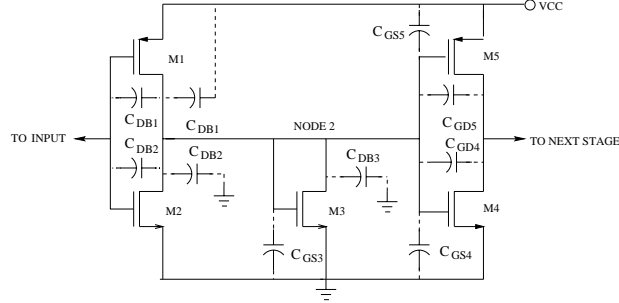
where

$$f_1(X(1), X(2)) = \frac{K_{pn}}{L_{effn}} X(1) [V_{GS} - V_{tn}] [1 + \lambda_n V_{GS}] + \frac{K_{pp}}{L_{effp}} X(2) [V_{DD} - V_{GS} - V_{tp}] [1 + \lambda_p (V_{DD} - V_{GS})] \quad (5)$$

$$f_2(X(1), X(2)) = \frac{K_{pn}}{L_{effn}} [V_{GS} - V_{tn}] [1 + \lambda_n V_{GS}] + \frac{K_{pn}}{2L_{effn}} X(1) \lambda_n [V_{GS} - V_{tn}]^2 + \frac{K_{pn}}{2L_{effn}} \lambda_n [V_{GS} - V_{tn}]^2 + \frac{K_{pp}}{2L_{effp}} X(2) \lambda_p [V_{DD} - V_{GS} - V_{tn}]^2 \quad (6)$$

The bandwidth of a single stage,  $BW_1$ , is given by (Figure 3):

$$BW_1 = \frac{g_{m3} + g_{ds1} + g_{ds2} + g_{ds3}}{C_{ND}} \quad (7)$$



**Figure 4.** The parasitic capacitances

The various contributions to the total parasitic capacitance,  $C_{ND}$ , are shown in Figure 4. The total capacitance,  $C_{ND}$ , which determine the bandwidth,  $BW_1$ , of the single stage is given by

$$C_{ND} = (C_{gs1} + C_{gs2} + C_{gs3}) + (C_{bd1} + C_{bd2} + C_{bd3}) + (A_1 + 1)(C_{gd1} + C_{gd2}) \quad (8)$$

where  $A_1$  is the gain of the single stage. The parasitic capacitances can be expressed in terms of the model parameters (table 1) and the geometry of the transistors.

PARAMETER	VALUE	PARAMETER	VALUE
$V_{tn}$	0.6V	$V_{tp}$	-0.8V
$DELTA_n$	0.7	$DELTA_p$	1
$LD_n$	0.1E-6m	$LD_p$	0.06E-6m
$K_{pn}$	1.1E-4A/V <sup>2</sup>	$K_{pp}$	4.06E-5A/V <sup>2</sup>
$C_{ox}$	2.03E-5F/m	$T_{ox}$	17E-9m
$C_{jn}$	4E-4F/m <sup>2</sup>	$C_{jp}$	4.8E-4F/m <sup>2</sup>
$C_{jsw_n}$	1.6E-10F/m	$C_{jsw_p}$	2E-10F/m
$C_{gdon}$	2.3E-10F/m	$C_{gdop}$	1.9E-10F/m
$K_{fn}$	3E-28	$K_{fp}$	5E-30

**Table 1.** LEVEL3: Berkeley Spice model

In terms of the model parameters, width ( $W$ ), and length ( $L$ ) of the transistors,  $C_{ND}$  can be expressed as

$$\begin{aligned} C_{ND} = & C_{ox}[LD_n + 0.67(L - 2 LD_n)][W_1 + W_3] \\ & + C_{ox}[LD_p + 0.67(L - 2 LD_p)]W_2 + C_{jn}(W_1 + W_3)L1 + C_{jp} W_2 L1 \\ & + 2 C_{jsw_n}[W_1 + W_3 + 2 L1] + 2 C_{jsw_p}[W_2 + L1](A_1 + 1)[C_{gdon} W_1 + C_{gdop} W_2] \end{aligned} \quad (9)$$

where,  $L1$  is the length of the drain and the source of each transistor. The source lengths and drain lengths of all transistors are fixed to the minimum of  $2.2\mu\text{m}$  as required by the design rules, minimizing the area and side-wall capacitances. From the equations (1, 4, 6, 7 and 9)

$$BW_1 = \frac{f_2(X(1), X(2))}{f_4(X(1), X(2))} \quad (10)$$

where  $f_2(X(1), X(2))$  is given by equation 6. From equation 9  $f_4(X(1), X(2))$  is approximately equal to

$$\begin{aligned}
f_4(X(1), X(2)) = & C_{ox}[LD_n + 0.67(L - 2 LD_n)][X(1) + 1] \\
& + C_{ox}[LD_p + 0.67(L - 2 LD_p)]X(2) + C_{jn}(X(1) + 1)L1 + C_{jp} X(2) L1 \\
& + 2 C_{jsw_n}[X(1) + 1] + 2 C_{jsw_p}[X(2)](A_1 + 1)[C_{g_{don}} X(1) + C_{g_{dop}} X(2)] \quad (11)
\end{aligned}$$

### 2.3. Nomograph

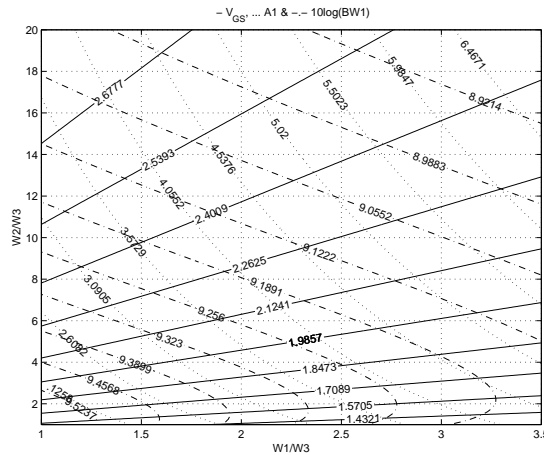


Figure 5. Nomograph

To assist in the detailed design and to allow the sensitivity of the performance to key parameters to be visualized graphically, a nomograph was developed as shown in Figure 5. The contours of Figure 5 show how the DC bias ( $V_{GS}$ ), the pole frequency ( $BW_1$ ), and the gain ( $A_1$ ) vary with the ratios  $X(1)(= W_1/W_3)$  and  $X(2)(= W_2/W_3)$ .  $V_{GS}$  can be expressed in terms of  $X(1)$  and  $X(2)$  as

$$V_{GS} = \frac{V_{DD} - V_{tp} + V_{tn} f_5(X(1), X(2))}{1 + f_5(X(1), X(2))} \quad (12)$$

where

$$f_5(X(1), X(2)) = \left\{ \frac{K_{pn} L_{effp}(X(1) + 1)}{K_{pp} L_{effn} X(2)} \right\}^{1/2} \quad (13)$$

Also, by consideration of the stability criterion outlined in section 2.2, the design is stable for all values of  $X(1)$  and  $X(2)$  for which  $10\log(BW_1) \geq 8.97$ .

### 2.4. Optimization

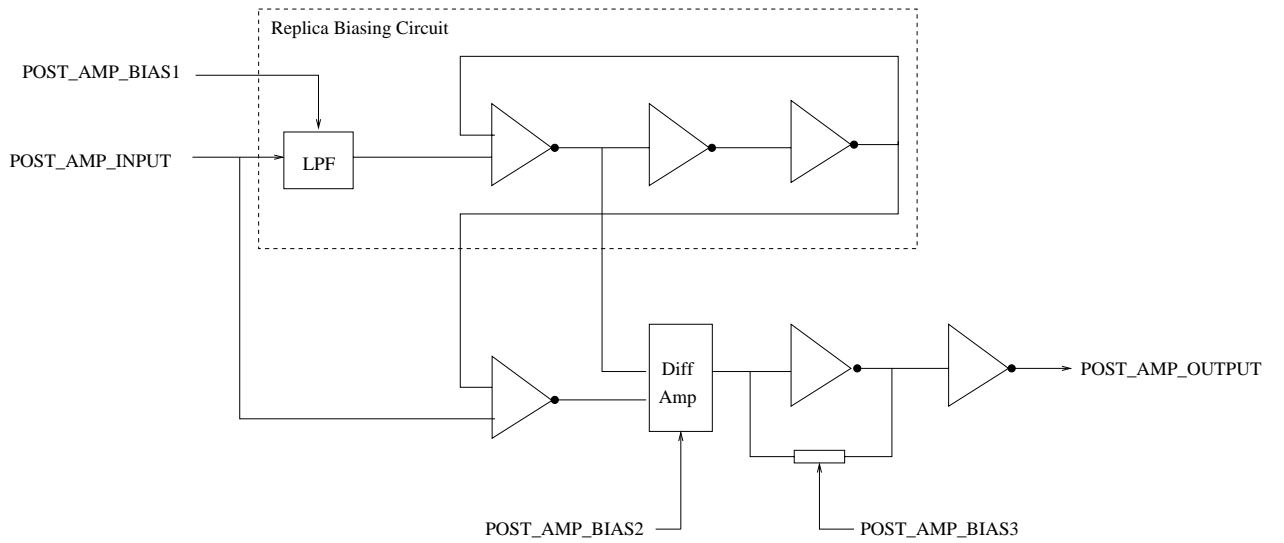
As mentioned before, the open loop gain should be maximized. To do so, a single stage is considered (Figure 2). It is loaded with the capacitance,  $C_{ND}$ , whose value depends on dimensions  $W_1, W_2$  and  $W_3$  as shown in Equation 9. The circuit has 7 degrees of freedom:  $V_{GS}, L_1, L_2, L_3, W_1, W_2$  and  $W_3$ . To achieve high speed and to limit the capacitances, the lengths of all the transistors are set to the minimum value ( $0.7\mu m$ ). As the amplifier is in a DC feed back configuration, the output voltage is equal to the input voltage resulting in an optimisation constraint. As  $A_1$  depends only on the ratio of transistor dimensions (Equation 4, 5 and 6), the exact value of  $W_3$  is not important. In the design the amplifier is assumed to drive an identical post amplifier. The optimisation constraints are:  $BW_1 > 939.93MHz, 2 \leq V_{GS} \leq 3$  and  $I_{D3} = I_{D1} + I_{D2}$ . The optimized single stage gain,  $A_1$ , is 5.2.

The receiver is designed to have a sensitivity of  $-30dBm$ . The PIN diode has a responsivity of  $1A/W$ .<sup>5</sup> To achieve the required sensitivity at a BER of  $10^{-9}$  the peak-to-peak input current ( $1\mu A$ ) should be 12 times the RMS noise.<sup>5,6</sup> The input transistors were sized<sup>5</sup> to achieve a  $BER < 10^{-9}$ .

## 2.5. Feedback resistor

The complete transimpedance amplifier consists of 3 stages with a feedback resistor (Figure 2). The photodiode is assumed to have a capacitance of  $10pF$ . According to equation 1, a feedback resistor of value  $10K\Omega$  may be used. In a CMOS process a  $10K\Omega$  resistor implemented in polysilicon will be extremely long and will introduce an unacceptable phase-shift at the bandwidth.<sup>7</sup> All other available resistor implementations (active area and well) also result in an unacceptable phase-shift. A better approach is to replace the resistor with a transistor in its linear region. As the transistor can be made very small for large resistance, the extra phase shift is limited. NMOS or PMOS transistors can be used for implementing the feedback resistor. However, the large signal behaviour of the NMOS is not acceptable.<sup>4</sup> The PMOS device does not suffer from this constraint and was chosen in preference for this purpose. With larger input currents, the output voltage is higher, raising  $V_{gs}$  for the PMOS, resulting in decrease in resistance and hence transimpedance. The PMOS device thus introduces dynamic signal compression which results in a larger tolerable dynamic range of the input signal.

## 3. POST AMPLIFIER

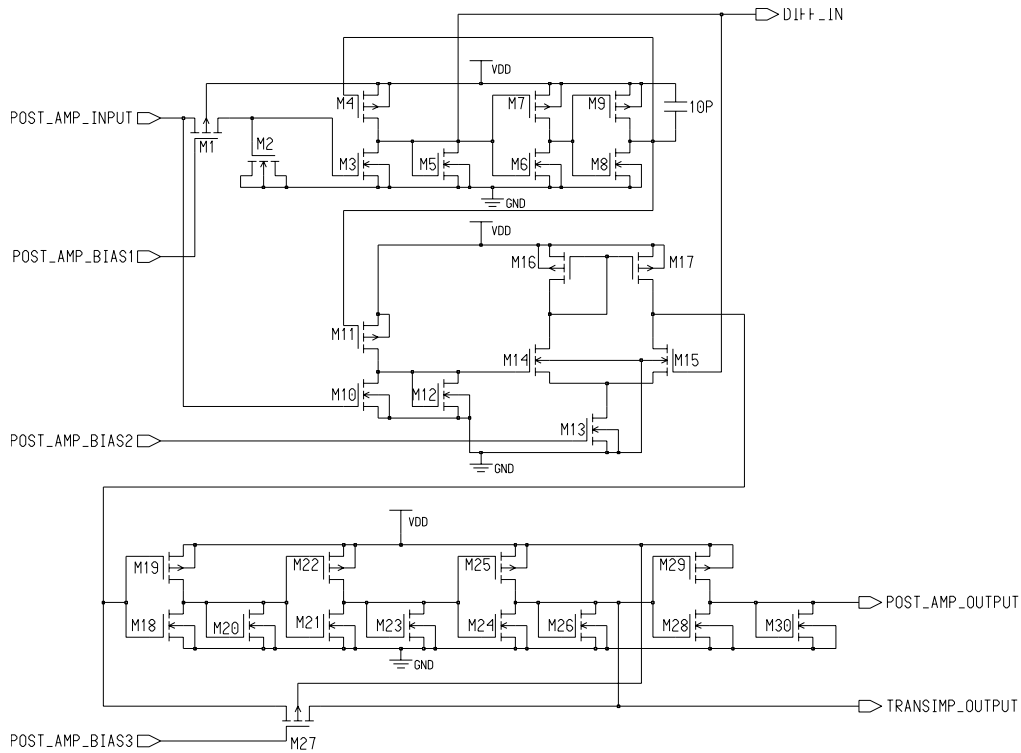


**Figure 6.** Post-Amplifier Circuit Block Diagram

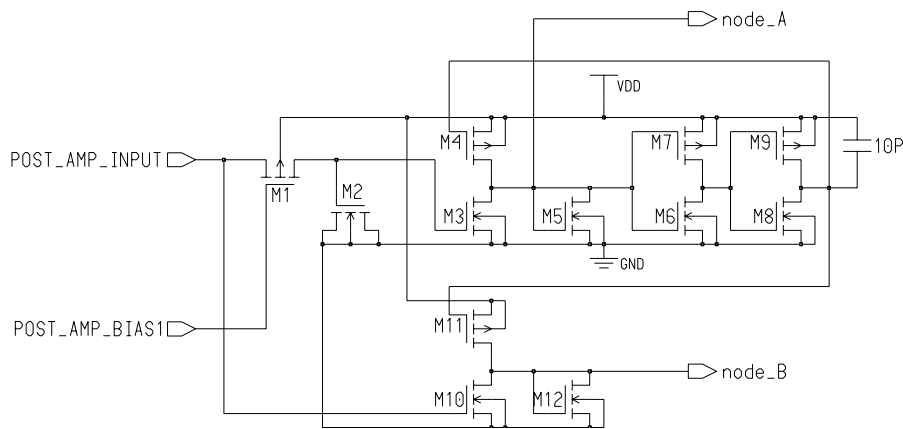
A block diagram and schematic of the full post-amplifier circuit can be found in Figures 6 and 7 respectively. The post-amplifier consists of several stages of amplification and a replica biasing circuit<sup>4</sup> to correctly bias the amplifier and achieve high tolerance to process variations. The replica biasing circuit is applied to the first stage of amplification to limit the pre-amplifier output to a DC level of 2.5V and provide input signal level detection. This technique is discussed in the next section. The second stage consists of a differential amplifier circuit with an externally controlled bias current, producing an output current that is amplified by the third stage of amplification, a transimpedance amplifier.

### 3.1. Replica Biasing Circuit

One of the most critical issues in the design of the post amplifier concerns biasing the pre-amplifier output to the threshold voltage of the inverter in the first stage. A replica biasing technique has been used and its circuit schematic along with the first stage of amplification (M10-12) can be found in Figure 8. Within the replica biasing circuit, an RC low pass filter is used to detect the mean value of the pre-amplifier output voltage signal. The low pass filter has a variable cut-off frequency that limits the lowest allowable signal frequency in the receiver and thus mitigates the  $1/f$  receiver noise considerably. This cut-off frequency can be set well below signal frequencies expected at the receiver input. The low pass filter resistor has been implemented using a PMOS transistor (M1) biased in the linear region by an external input signal, POST\_AMP\_BIAS1, and is used to control the cut-off frequency of the low pass filter.



**Figure 7.** Post-Amplifier Circuit Schematic



**Figure 8.** Replica Biasing Circuit Schematic

The gate capacitance of transistor (M2) gives a capacitance value suitable for the low pass filter. This approach greatly reduces the amount of silicon area necessary to implement a capacitance value of 5pF in the 0.7um CMOS process technology chosen for fabrication of this design. The basic operation of the biasing circuit involves using a feedback loop (M6-8) to set the voltage at node A (Figure 8) to the threshold of an inverter. The drain current of transistor M4 is mirrored to transistor M11 of the first stage of amplification. As a result, node B (Figure 8) is set to the same voltage as node A. One of several key requirements for this approach involves matching the dimensions of transistors M3/4 and M10/11 in order to maintain high performance and sensitivity. In addition, a diode coupled NMOS transistor (M5, M12) is added primarily to reduce Miller effect and loading by the post-amplifier on the preceding pre-amplifier circuit.

### 3.2. Stages of Amplification

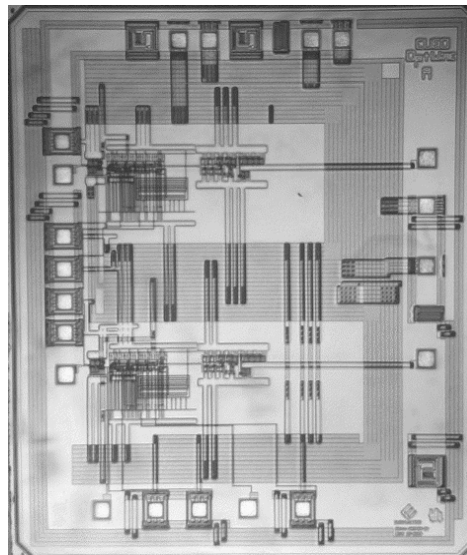
The traditional approach to designing a post-amplifier circuit involves using an inverter string biased in the high gain region. In order to achieve high performance independent of process variations, the output of the pre-amplifier stage must provide a voltage swing of at least 100mV. Variations in transistor dimensions and parameters such as threshold voltage are highly dependent on the technology being used for circuit fabrication. These variations (Table 2) can cause the output voltage swing of an inverter in the string to shift from the high gain region and degrade performance.

	NMOS	PMOS
Typical	0.76V	-1
Slow	0.89V	-1.12V
Fast	0.64	-0.87

**Table 2.** Level 53 SPICE Models for Alcatel 0.7 $\mu$ m Process: Threshold Voltage Variation

A different approach has been examined in this work. A transconductance stage consisting of a differential amplifier circuit is followed by a transimpedance amplifier for post-amplification. The differential amplifier stage includes a p-channel current mirror (M16-17) and an NMOS current sourcing transistor (M13) providing a variable supply current, controlled by POST\_AMP\_BIAS2. To maintain proper DC biasing at the output of the differential amplifier, a constant supply current is necessary. Process variations can potentially change the supply current, and therefore, an external bias has been implemented. The differential amplifier is also biased by the replica biasing circuit.

The output current from the differential amplifier stage is further amplified by the third post-amplifier stage, consisting of a 3-stage transimpedance feedback amplifier (M18-27) similar to the pre-amplifier circuit discussed in Section 2. The transimpedance feedback amplifier gives sufficient bandwidth and exhibits a very high tolerance to process variations. The feedback resistor for this third stage has been implemented with a PMOS transistor (M27) biased in the linear region by an external input signal, POST\_AMP\_BIAS3. An output buffer (M28-30) is used to provide rail-to-rail voltage swing.



**Figure 9.** Microphotograph



#### 4. REALIZATION OF COMPLETE RECEIVER

The optical receiver IC has been realized using the Alcatel Microelectronics CMOS 0.7 $\mu$ m process technology. The IC consists of two complete and functionally identical receiver test structures. A microphotograph of the chip is shown in Figure 9. The first structure, RECEIVER1 (top), is intended for high performance testing at 310Mb/s (155Mbps Manchester coded). Within the second structure, RECEIVER2 (bottom), various nodes within the receiver circuit have been bonded out to I/O pads to allow monitoring DC voltages and to observe the dynamic behaviour of the receiver at intermediate frequencies. These nodes are labelled in Figure 7 as POST\_AMP\_INPUT (output of pre-amplifier circuit), TRANSIMP\_OUTPUT, and POST\_AMP\_OUTPUT. Except for the photodiode detector and decoupling capacitors, the receiver chip requires no external circuit components.

In this implementation, separate power/ground supplies have been used for the analog and digital circuitry. This precaution has been taken to prevent noise coupling from switching (digital) circuitry onto sensitive (analog) circuitry through the low resistive paths to the power supply.<sup>8</sup>

#### 5. RESULTS

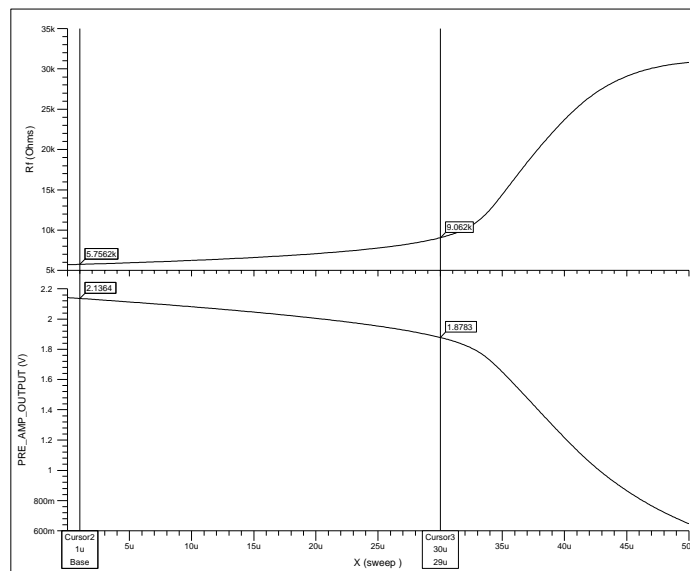
The PIN-diode is modelled as a diode with a depletion capacitance of 10pF in parallel with a current source. Simulations were carried out in the Mentor Graphics IC Station suite.

##### 5.1. Transimpedance characteristics

Simulation result show a transimpedance of 82.5dB and a  $-3dB$  bandwidth of 217MHz. The open loop gain of the pre-amplifier is 80.6, and the gain of single stage, A1 is 4.85. These values were used to determine the sizes of the transistors of the first stage (M1, M2 and M3), in order to optimise for noise.

The stability condition requires that the total open loop phase shift of the amplifier at the transimpedance bandwidth be less than  $45^\circ$ . Simulation results show a phase shift of  $27.4^\circ$ , giving enough phase margin to account for additional phase shift which may result from the parasitic capacitances and the loading of the next stage.

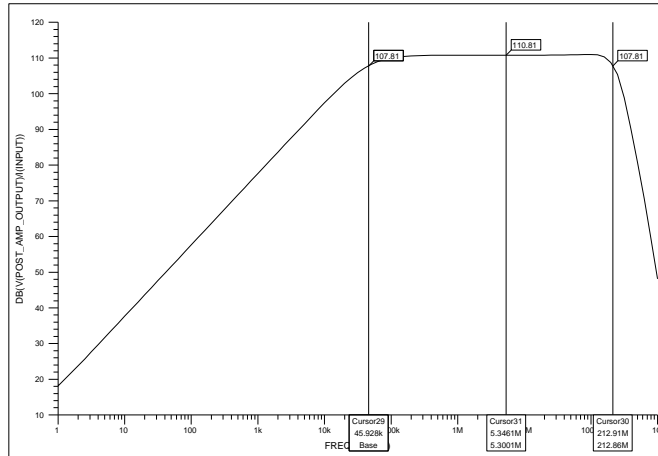
##### 5.2. Dynamic Range



**Figure 10.** Dynamic range: Feedback Resistance Rf (top), Pre-amplifier Output Voltage (bottom)

Figure (10) shows the variation in the output voltage for various values of input DC current. Only for input currents greater than  $35\mu A$  does the PMOS feedback transistor begin to saturate, thus providing a good dynamic range.

### 5.3. Receiver Frequency Analysis

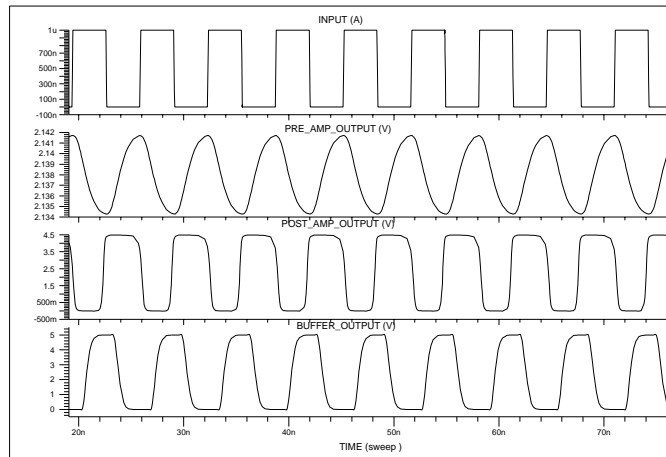


**Figure 11.** Receiver Transfer Function:  $DB(V(POST\_AMP\_OUTPUT)/I(INPUT))$

The transfer function from the pre-amplifier input current to the post-amplifier output voltage can be found in Figure 11. The lower cut-off frequency ( $45\text{KHz}$ ) set by the replica biasing circuit has a significant impact on the  $1/f$  noise characteristics of the receiver circuit. These low frequency characteristics are not a significant limitation to performance, as the data is Manchester coded to limit the low frequency content.

### 5.4. Receiver Transient Analysis

Four waveforms are shown in Figure 12 as a result of simulation under typical conditions at 310 Mb/s: the input current signal, pre-amplifier output voltage, post-amplifier output voltage, and the final buffer output voltage. Two parasitic elements have been included in this simulation: (1) photodetector capacitance ( $4\text{pF}$ ) at receiver input, and (2) output load of  $10\text{pF}$  (interconnect, pad, and package capacitance).



**Figure 12.** Receiver Circuit Transient Analysis:(top to bottom) input current signal, pre-amplifier output voltage, post-amplifier output voltage, final buffer output voltage.

## 6. CONCLUSIONS

The future of optical wireless LANs will rest on the ability to design, develop, and implement high performance integrated circuits. In this dissertation, a CMOS optical receiver chip has been designed and developed for implementation in to a fully integrated optical wireless LAN application.

In order to simplify the design procedure of pre-amp a nomograph approach has been developed. The great advantage of using the nomograph is that it facilitates the sizing of the transistors for a particular bandwidth. In addition, use of this approach facilitates clearer visualization of the complex design tradeoffs. Note that different nomographs are required for different amplifier configurations and device technologies, but it is comparatively simple to generate these using a suitable computer program.

The noise performance of a CMOS transimpedance amplifier can be improved by increasing the sizing of the first stage of the amplifier. The nomograph shows how the sizing of the first stage of the amplifier can be adjusted without affecting the stability.

The post-amplifier circuit includes a replica biasing technique for proper biasing of the stages of amplification and to detect the mean of the received signal. The inherent low-pass filter in the replica biasing circuit provides a lower cut-off frequency of 40 KHz to filter  $1/f$  noise present in the receiver. Simulations confirm operation of the receiver circuit up to a bit rate of 310 Mb/s (155 Mb/s Manchester coded).

## ACKNOWLEDGMENTS

The authors wish to thank the Engineering and Physical Sciences Research Council (EPSRC), the Cambridge Commonwealth Trust, and the British Marshall Commission for their financial support.

## REFERENCES

1. S. Greaves, P. Nicholls, D. Wisely, and R. Unwin, "Optical wireless video distribution," *SPIE* **2601**, pp. 280–285, 1995.
2. M. McCullagh and D. Wisely, "155 Mbit/s optical wireless link using a bootstrapped APD receiver," *Electronics Letters* **30**, pp. 430–431, March 1994.
3. P. Nicholls, R. Unwin, and K. Dalton, "A 10Mb/s optical wireless ethernet - practical results," *SPIE* **2601**, pp. 294–304, 1995.
4. M. Ingels, G. V. der Plas, J. Crols, and M. Steyaert, "A CMOS 18 THzOhm 240Mb/s transimpedance amplifier and 155Mb/s LED-driver for low cost optical fiber links," *IEEE Journal of Solid-State Circuits* **29**, pp. 1552–1559, December 1994.
5. V. A. Lalithambika, *Master of Philosophy dissertation; Application of VLSI to Wireless Networks*. University of Cambridge, 1999.
6. M.-S. Park, C.-S. Shim, and M.-H. Kang, "Analysis of sensitivity degradation caused by the flicker noise of GaAs-MESFETs in fiber-optic receivers.," *Journal of Light Wave Technology* **6**, pp. 660–667, May 1988.
7. G. F. Williams, *Topics in lightwave transmission systems*, ch. 2. Lightwave Receivers. Academic Press, 1991.
8. V. M. Joyner, *Master of Philosophy dissertation; Integrated Circuit Design for Wireless Network Receivers*. University of Cambridge, 2000.