

Homework #1

EE 194: Advanced VLSI Spring 2018

Problems

1. Consider a long wire with $RC=100\text{ps}$. How will R , C and RC change after one generation of scaling?
2. Assume a wire with $RC=100\text{ps}$. (a) If we double the wire length, how does RC change? (b) What if we instead double the width? (c) The height (specifically, the height of the wire itself, not the inter-layer spacing)?
3. Let's try to improve the delay of this 100ps wire. (a) If we broke the wire in half and added a buffer of delay 10ps , what would the delay now be? (b) Into three pieces? (c) Into quarters? (d) We mentioned in class that wire RC varies quadratically with wire length. Thus, driving a wire twice as far would take 4 times as long, and driving a wire 10 times as far would take 100 times as long. In general, if you are allowed to add buffers, and the buffers have substantially smaller delay than the wire, is there a way that we can do much better than this quadratic dependence for longer distances?
4. One way to improve wire R might be to make the metal layers taller, increasing the metal height. Assume that we double the metal height H , while leaving the inter-layer metal spacing (what the class slides called $H_{\text{inter-layer}}$) unchanged. How would that affect wire R ? How would it affect C_{area} ? How would it affect C_{lateral} (the capacitance between adjacent wires)? Would $R(C_{\text{area}}+C_{\text{lateral}})$ get larger or smaller as a result? Note that making wires very tall and skinny also makes them difficult to manufacture reliably.
5. A circuit has $P_{\text{dyn}}=100\text{mW}$ and $P_{\text{static}}=20\text{mW}$. A calculation takes 1000 cycles at $T_{\text{cycle}}=1\text{ns}$. (a) What is the total energy in nJ ? (b) If we halve the clock frequency, what happens to the total power (static plus dynamic) for the calculation? (c) To the total energy?
6. The same circuit (which is running at 1V) has a total switching capacitance of 1nF (i.e., 10^{-9}Farad). (a) What is its activity factor? (b) Assume now that the circuit has two clocks, each one controlling half of the logic. If we gate off one of the two clocks, we eliminate all switching of all of the logic in its half of the circuit. Assume that this also removes $\frac{1}{4}$ of the switching in the other clock's logic (e.g., because some inputs to the other half are now quiescent). What is the new dynamic power?