Homework #5 (DVFS)

Problem #1. Consider a chip that has DVFS and can choose between running at 1 GHz/1V or 1.5GHz/1.5V. Assume that:

- there is a constant leakage power of 5W (in reality, the leakage power would drop substantially as we lower the supply voltage)
- the dynamic power at the 1 GHz/1V operating point is 20W, and in general is given by $C_{\text{eff}}V^2f$.

What is the total power at the 1.5GHz frequency? If a particular calculation takes 1B cycles, how much energy do we save by running at 1GHz/1V rather than 1.5GHz/1.5V?

***Problem #2*.** Consider the same chip from problem #1, but this time assume for simplicity that leakage power is zero.

A particular calculation takes 1B cycles. It would thus take 1 sec at 1GHz and .5 sec at 2GHz. Of course, we save energy if we can allow the full one second and run at the lower frequency and voltage. How much energy do we require at 1 second and at .5 seconds?

In our case, a customer requires that the calculation finish in .75 seconds. What frequency would we have to run at to finish in this amount of time? Assuming for simplicity that frequency is simply proportional to voltage, what voltage would we need? How much energy would we need at this voltage and frequency?

Having more V/F points requires more test time, and is not always cost effective. Another strategy for this customer, instead of adding a new V/F point, would be “dithering.” We run part of the computation at 1GHz and part at 1.5 GHz. How many cycles of the 1B must we run at 1.5GHz in this case, and how many can go at 1GHz? How much energy would the computation cost in this case?

Problem #3. We mentioned in class that switching a PLL to a new frequency does not happen instantaneously, and that it can be difficult to design circuits that can run while the clock is switching. There are several approaches that have been taken:

- Look at the paper "Dynamic Frequency-Switching Clock System on A Quad-Core Itanium Processor" from 2009 ISSCC. What solution do they use? What are its pros and cons?
- The solution from the 2009 ISSCC paper is not used very widely any more, since more PLLs are capable of transitioning smoothly from one frequency to another (without generating runt clock pulses or any undesirable clock artifacts). However, the transition of course does not happen instantaneously; it stills needs a nontrivial amount of time, and the PLL outputs a LOCK signal that goes high when it has locked to the new frequency. Assume that we have this type of PLL. Similarly, assume we have a power supply that can smoothly transition from one voltage to another, and implement a STABLE signal when done. This all sounds good; however, when we switch to a new, higher frequency and voltage, and both V and F ramp higher, we risk having intermediate points in time when frequency has ramped faster than voltage, and the circuit thus does not meet critical paths for a short time and fails. Can you think of a simple solution for dealing with this? How about a similar solution for transitioning to a lower V and F? The solution does not have to be particularly speedy, but it does have to work reliably.

Please turn in your assignment via the Provide cgi interface. You can use any reasonable format (including writing your answers by hand and taking a picture of the page with your phone).