# EE194: Advanced VLSI Design
Spring 2018

Instructor: Joel Grodstein (joel.grodstein@tufts.edu)
Meeting time: Mon/Wed 4:30-5:45pm

***Course description***: *Advanced VLSI* is the next VLSI class after EE103 (Introduction to VLSI Design). We will study roughly half a dozen different topics detailed below, including process scaling, static-timing analysis and speed binning, clocking, validation, DVFS, latching and scan, and future directions for VLSI.

***Expected course outcomes***:

- students will learn enough about VLSI to appreciate the challenges of designing chips that, each year, encompass more and more complexity and become more and more ubiquitous in our lives.
- students will learn learn not only about design, but also about validation and some areas of post-silicon testing.

***Textbook***: none. The material will be covered mainly by lectures, and partially by reading research papers.

***Prerequisites***: EE103, or graduate standing, or consent of the instructor. The class will assume that you understand most of the material in EE103.

***Guest lecturer***: we will most likely have a guest lecturer from Cavium, talking about verification. We will cover this topic in the class as well.

***Course structure***: the course will cover half a dozen or so topics in VLSI. Each topic will have roughly two weeks of lectures. There will then be an assignment; typically a paper-and-pencil homework. Some of the assignments may be replaced by a short in-person oral quiz.

There will be little (if any) use of commercial CAD tools.

***Tests, projects, grading and logistics***. The class grade will mostly be determined by the homeworks. We may have a final exam, depending on how the class progresses. Homework will be available on the class web page, and should be turned in via *provide*. Grades will be returned on Trunk.

***Late assignments***: each student will be allocated five late days per semester that can be used for homework assignments and course projects. Please make a note on top of the assignment if you would like to use a late day. After the allocated late days have been exhausted, the grade on a late assignment will be penalized by 10% per day.

***Tentative schedule of course material:***
The potential topics are listed below. We will cover some subset of them, depending on the pace of the class and on student interest.

- *The physics of process scaling*. Over the last 40 years, Moore's Law has driven the semiconductor industry into a gigantic economic force; VLSI is the driver behind smart phones and is equally present in refrigerators. What is the physics behind this? What is causing it to come to an end? How did predictions of heat dissipation on the scale of a nuclear reactor not come to be?
- *Static-timing analysis*. Faster is (usually) better. We will learn about why we want VLSI chips to run faster (not just the obvious reason!), and about the constraints that our circuits must obey for latches, flops and conditional clocks. We will also talk about

floorplanning to minimize timing-closure effort. We will also talk about how static timing interacts with post-silicon speed testing and binning.

- *Clocking*. Chips need clocks. Many designers merely assume that perfect clocks somehow arrive at their doorstep – in reality, generating good clocks without excessive power is a difficult process. We will learn more about how they work and how clock skew is controlled.
- *Validation*. In universities, we typically assume that designing a chip is the hard part, and rarely build our chips to see if they really work. In industry, RTL validation is the fastest-growing area for VLSI jobs. We will learn how validation is done, and do some ourselves.
- *DVFS*. Discrete Voltage and Frequency Switching is a common means of conserving power by changing voltage and frequency on the fly to match them with the actual computing load. We will also discuss how DVFS affects static timing and post-silicon speed binning.
- *Latching and scan*. We will learn about flops vs latches, and what is inside of both of them. We will also learn the basics of scan, which is the way that the overwhelming majority of chips are tested – and how scan interacts with normal design.
- *Future technology*: dark silicon, timed digital, and computing with bacteria. As Moore's Law reaches the end of its useful life, it is not clear where the VLSI industry will go in the next 15 years. We will discuss several interesting possibilities, as well as reading research papers.

***Potential research papers to read:***

- The future of microprocessors, Shekhar Borkar 2011
- Computational sprinting, 2011
- Next Generation Intel Core Micro-Architecture (Nehalem) Clocking, JSSC 2009

***Collaboration policy*:** Learning is a creative process. Individuals must understand problems and discover paths to their solutions. During this time, discussions with friends and colleagues are encouraged—you will do much better in the course, and at Tufts, if you find people with whom you regularly discuss problems. But those discussions should take place in English, not in code. If you start communicating in code, you're breaking the rules. When you reach the coding stage, therefore, group discussions are no longer appropriate. Each program, unless explicitly assigned as a pair problem, must be entirely your own work. Do not, under any circumstances, permit any other student to see any part of your program, and do not permit yourself to see any part of another student's program. In particular, you may not test or debug another student's code, nor may you have another student test or debug your code. (If you can't get code to work, consult a teaching assistant or the instructor.) Using another's code in any form or writing code for use by another violates the University's academic regulations. Do not, under any circumstances, post a public question to Piazza that contains any part of your code. Private questions directed to the instructors are OK. Suspected violations will be reported to the University's Judicial Officer for investigation and adjudication. Be careful! As described in the handbook on academic integrity, the penalties for violation can be severe. A single bad decision made in a moment of weakness could lead to a permanent blot on your academic record. The same standards apply to all homework assignments; work you submit under your name must be entirely your own work. Always acknowledge those with whom you discuss problems!

Suspected violations will be reported to the University's Judicial Officer for investigation and adjudication. Again, be careful!

***Additional resources*:**
Tufts University values the diversity of our students, staff, and faculty, and recognizes the important contribution each student makes to our unique community. Tufts is committed to providing equal access and support to all qualified students through the provision of reasonable accommodations so that each student may fully participate in the Tufts experience. If you have a disability that requires reasonable accommodations, please contact the Student Accessibility Services office at Accessibility@tufts.edu or 617-627-4539 to make an appointment with an SAS representative to determine appropriate accommodations. Please be aware that accommodations cannot be enacted retroactively, making timeliness a critical aspect for their provision. Tufts and the teaching staff strive to create a learning environment that is welcoming to students of all backgrounds. If you feel unwelcome for any reason, please let us know so we can work to make things better. You can let us know by talking to anyone on the teaching staff. If you feel uncomfortable talking to members of the teaching staff, consider reaching out to your academic advisor, the department chair, or your dean.